Technical Information Manual

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MOD. N840-N841
8-16 CHANNEL
LEADING EDGE
DISCRIMINATOR

NPO:
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CAEN declines all responsibility for damages or injuries caused by an improper use of the Modules due to negligence on behalf of the User. It is strongly recommended to read thoroughly the CAEN User's Manual before any kind of operation.

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CAEN reserves the right to change partially or entirely the contents of this Manual at any time and without giving any notice.

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1. General description

1.1. Functional description

The CAEN Model N841 is a 16 CHANNEL LEADING EDGE DISCRIMINATOR housed in a single width NIM module.

The module accepts 16 negative inputs and produces 16 NIM outputs + 16 /NIM outputs (complementary) on 48 front panel LEMO 00 connectors (NIM outputs are provided with a Fan-Out of two); a functional block diagram is shown in Fig. 1.1.

A 8 Channel version, the CAEN Model N840, sharing the same functional features with the 16 Channel Model N841, is also available.

The Pulse Forming Stage of the discriminator produces an output pulse whose width is adjustable in a range from 5 ns to 40 ns.

Each channel can work both in Updating and Non-Updating mode according to on-board jumpers position.

The discriminator thresholds are settable in a range from -1 mV to -255 mV (1 mV step), via an 8-bit DAC.

The back panel houses VETO and TEST inputs, the logical OR output (the relevant front panel “OR” LED lights up if at least one channel is over threshold) and the Current Sum (Σ) output, which generates a current proportional to the input multiplicity, i.e. to the number of channels over threshold, at a rate of -1.0 mA per hit (-50 mV per hit into a 50 Ohm load) ±20%. A four digit LED display provides information on the module’s status.

1.2. Block diagram

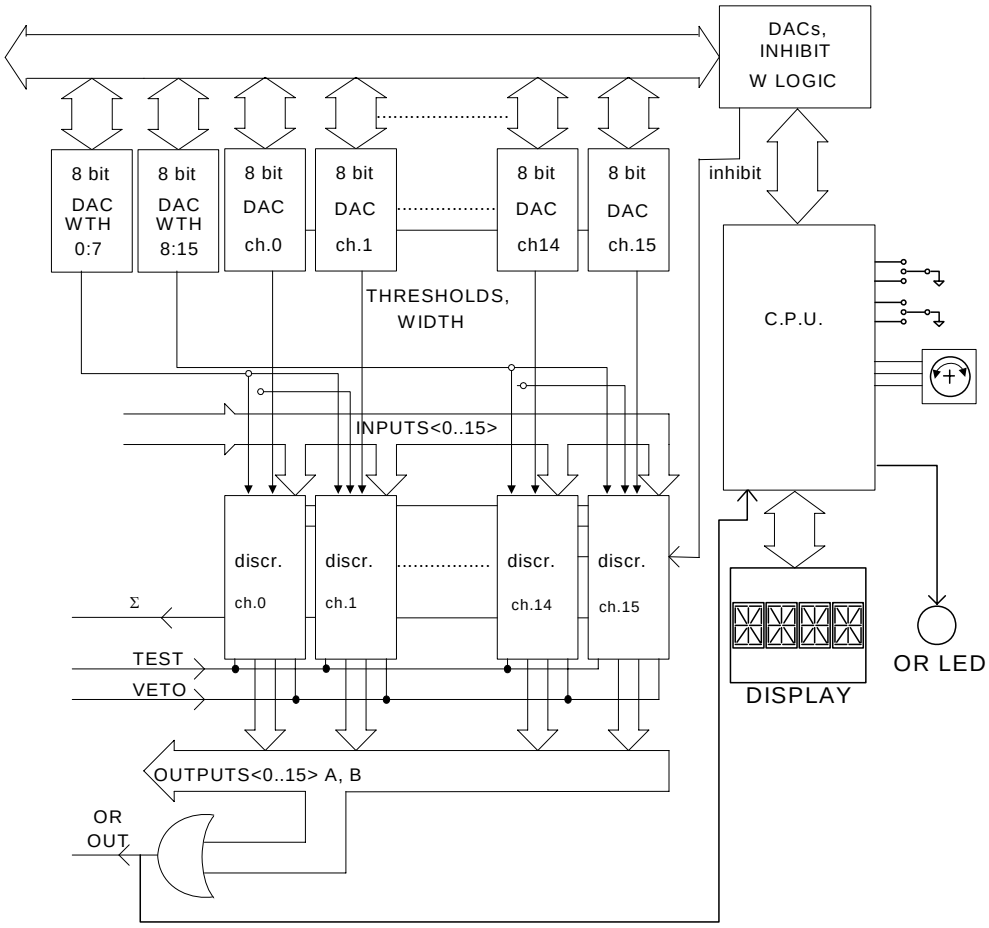


Fig. 1.1: Mod. N841 Block Diagram (16 Channel)

2. Technical Specifications

2.1. Packaging

The Model N840-N841 is housed in a 1U-wide NIM unit.

2.2. Power requirements

The power requirements of the Mod. N840-N841 are as follows:

Table 2.1: Power requirements

Power supply	N840	N841
+ 12 V	50 mA	60 mA
- 12 V	20 mA	30 mA
+ 6 V	370 mA	600 mA
- 6 V	1.9 A	3.45 A

2.3. Front and back panel

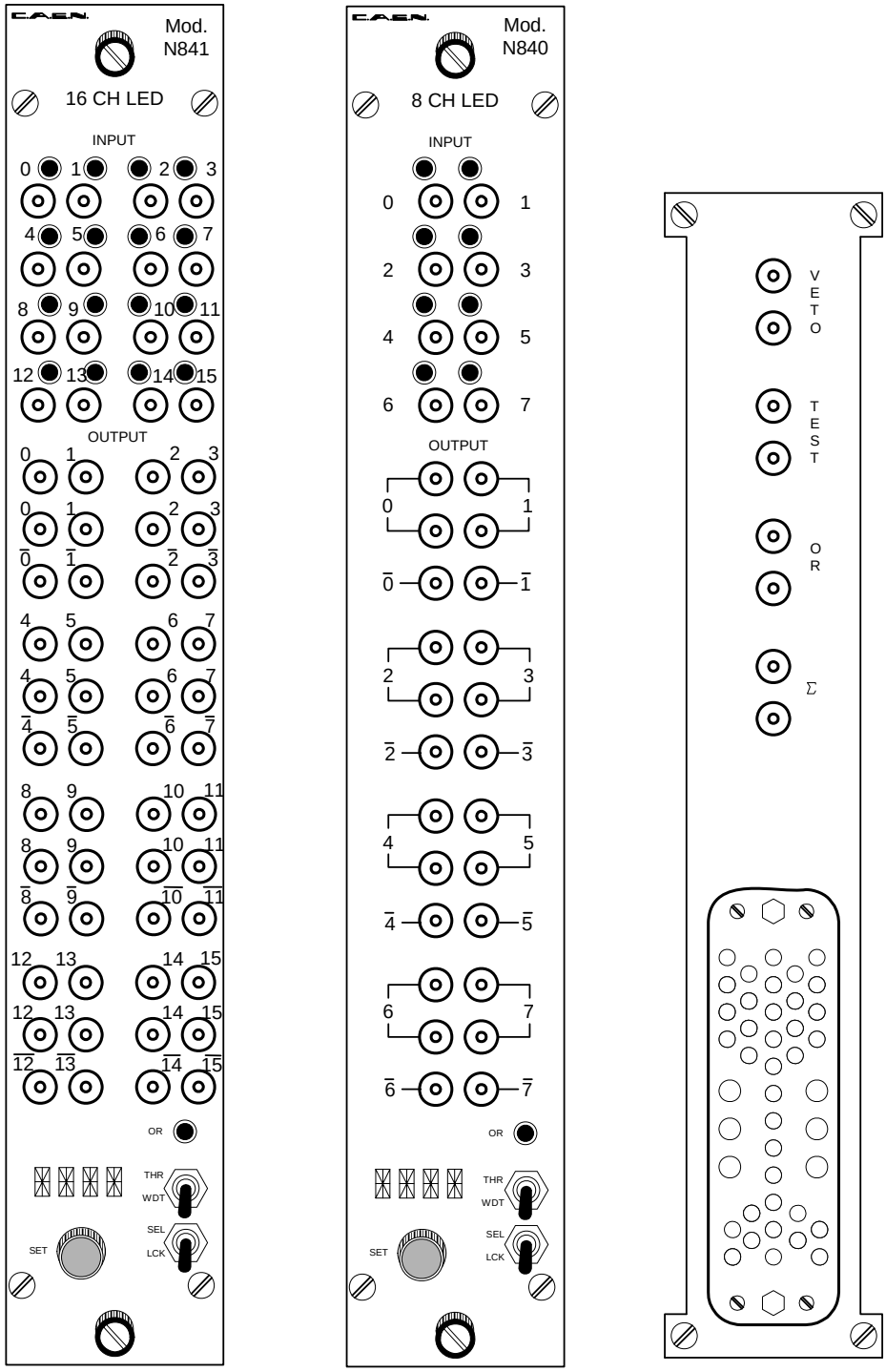


Fig. 2.1: Mod. N841-N840 front panel and back panel

2.4. Input/Output connections

The location of the Mod. N840-N841 connectors is shown in Fig. 2.1. Their function and electromechanical specifications are listed in the following subsections and are referred to the Mod. N841 (the Mod. N840 features specified between [ ]).

2.4.1. INPUT features

INPUT CHANNELS:

Mechanical specifications:
16 [8] LEMO 00 type connectors.
Electrical specifications:
negative polarity, 50 Ohm impedance; DC coupling; maximum ratings: -5 V; maximum input frequency: 110 MHz (updating), 80 MHz (non-updating). Min. detectable signal: -5 mV.

VETO INPUT:

Mechanical specifications:
2 bridged LEMO 00 type connectors.
Electrical specifications:
standard NIM signal, high impedance, 15 ns minimum FWHM; leading edge of the VETO signal must precede of at least 6 ns the leading edge of the input and overlap completely the input signal; acts on all signals.

TEST INPUT:

Mechanical specifications:
2 bridged LEMO 00 type connectors.
Electrical specifications:
standard NIM signal, high impedance, 12 ns minimum FWHM, 40 MHz maximum frequency. Test/Outptut delay: 11 ns

2.4.2. OUTPUT features

OUTPUT CHANNELS:

Mechanical specifications:
48 [24] (32 [16] Fan-Out of two for OUT and 16 [8] single for /OUT) LEMO 00 connectors.
Electrical specifications:
NIM level on 50 Ohm impedance; pulse width adjustment: Out: 5 ÷ 40 ns, /Out: 6 ÷ 41 ns; Input/Output delay: 9 ns

OR OUTPUT:

Mechanical specifications:
2 LEMO 00 type connectors, Fan-Out of two.
Electrical specifications:
standard NIM signal, 50 Ω impedance, 10 ns minimum FWHM, 30 MHz maximum frequency.

Σ OUTPUT:

Mechanical specifications:
2 bridged LEMO 00 type connectors.
Electrical specifications:
current output (-1 mA ± 20% per hit), high impedance. 15 ns minimum FWHM, 30 MHz maximum frequency.

2.5. Other components

2.5.1. Displays

The front panel hosts the following LEDs:

INPUT
Type: 16 [8] red LEDs
Function: channel selected; they light up when the channels are being programmed (SEL mode) and when they are inhibited (LCK mode)

OR
Type: 1 green LED
Function: it lights up if at least one output signal is present.

4 DIGIT DISPLAY
Type: 4 digit red LED display
Function: it indicates the channels' status and programmed parameters' values

2.5.2. Front panel switches

UPPER SWITCH
Function: it allows to select the parameter which must be programmed

LOWER SWITCH
Function: it allows to select the channel/block which must be programmed (SEL mode), and to "freeze" the programmed values (LCK mode)

2.5.3. Rotary handle

Function: it allows to set the value of the parameter which is being programmed

2.5.4. Jumpers

MODE SELECTION JUMPERS
Function: these 3-position jumpers allow to set the working mode (Updating or Non-Updating). Please refer to Fig. 2.2 for the jumpers location on the N840-N841 boards.

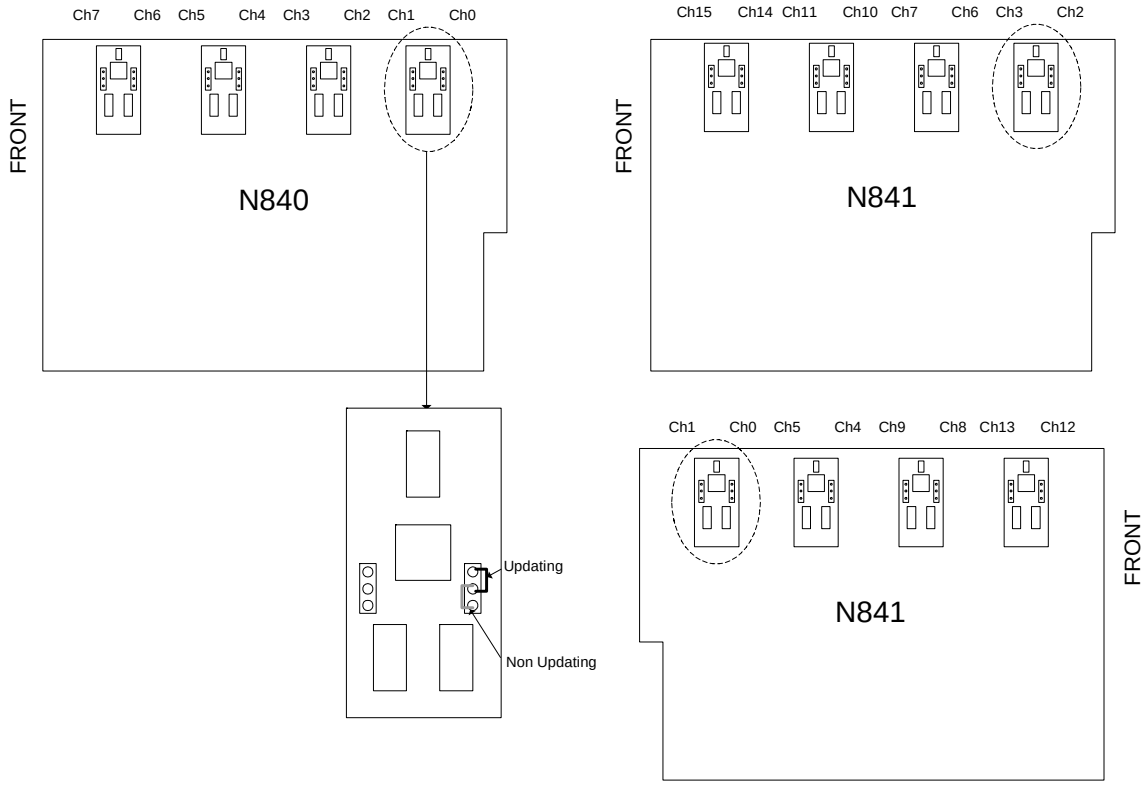


Fig. 2.2: Jumpers location

2.6. Technical specification table

Table 2.2: Technical specification table

Features referred to Mod. N841 (Mod. N840 features specified between [ ])

Packaging	1U-wide NIM unit
Threshold range	-1 mV to -255 mV (1 mV step)
Input Channels	16 [8] inputs, negative polarity, DC coupling
Input Impedance	50 Ω
Reflections	<4% for input pulses with a 2 ns rise time
Interchannel isolation	>44 dB
Max Input voltage	-5 V
Min. detectable signal	-5 mV
Max input frequency	110 MHz (Updating mode) 80 MHz (Non Updating mode)
Double Pulse Resolution	7 ns (Updating mode), 12 ns (Non Updating mode)
Test Input	NIM signal; High impedance; Min. FWHM: 12 ns; Max. frequency: 40 MHz
Veto Input	NIM signal; High impedance; Min. FWHM: 15 ns
Output channels	32 [16] NIM (Fan-Out of 2) + 16 [8] /NIM (single), 50 Ω Impedance
Output Width	Out: 5 ÷ 40 ns /Out: 6 ÷ 41 ns
Output Rise/Fall Time	Out: < 1.2 ns; /Out: < 2.5 ns
Input/output delay	9 ns
Test Input/output delay	11 ns
Or Output	NIM signal; 50 Ω impedance Max. frequency: 30 MHz; Min. FWHM: 10 ns
Σ Output	-1 mA ± 20% per hit; high impedance Max. frequency: 30 MHz; Min. FWHM: 15 ns

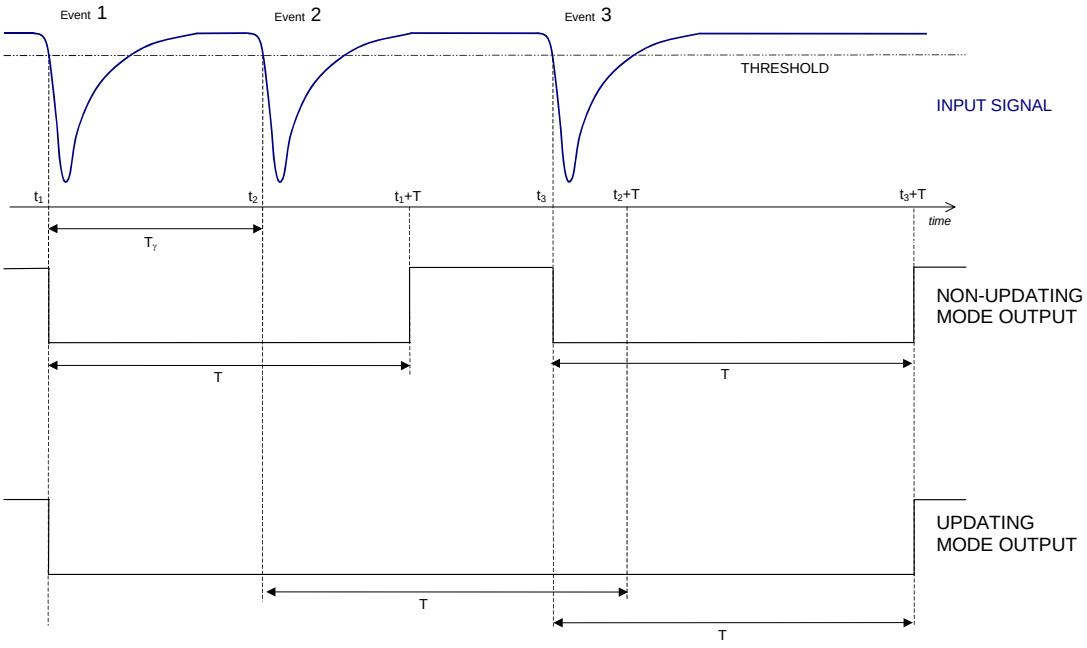
3. Operating Modes

3.1. Updating and Non-Updating mode setting

Each channel of the Mod. N840-N841 may provide an Updated (retriggerable) or a Non-Updated (not retriggerable) output. Output mode selection is performed, individually for each channel, via jumpers, as shown in Fig 2.2.

Non-Updating output mode: an input pulse over threshold occurring at t_1 (event 1 in fig. 3.1) sets the channel output active for the programmed duration[1] T (T=5÷40 ns). Any event over threshold occurring at t, with $t_1<t<t_1+T$, will be ignored.

Updating output mode: input pulse over threshold occurring at t_1 (event 1 in fig. 3.1) sets output active for the programmed duration[1] T (T=5÷40 ns). Any input event over threshold for $t_e<t_1+T$, will restart the pulse forming stage forcing the output to active value until instant t_e+T.



T	5÷40 ns	(programmable)
T_γ min	7ns Double Pulse Resolution (updating)	
	12ns Double Pulse Resolution (non-updating)	

Fig. 3.1: N840-N841 Updating and Non-Updating mode

[1] Pulse duration ranges from 6 to 41 ns for negated outputs (/Out).

3.2. Power ON Status

At Power ON the values of all the module's parameters are those programmed before the last turning off. If one parameter's value is meaningless, the unit sets it at half of its range.

3.3. Back panel signals

Some operations can be performed via two external NIM input signals:

- TEST: an input signal sent through this connector triggers all the enabled channels at once. This feature allows a complete test of the module without removing any input cable as well as it allows generation of a pattern of pulses suitable to test any following electronics.
- VETO: an input signal sent through this connector allows vetoing of all channels simultaneously. A veto pulse of width T will veto the input during this time T. Its leading edge must precede the output leading edge by at least 6 ns and overlap completely the input signal. VETO does not affect the TEST signal.

Each one of these high impedance inputs is provided via two bridged connectors (placed on the board's back panel) for daisy chaining.

Note that since these are high impedance inputs, the chain has thus to be terminated on 50 Ω on the last module; the same is required whenever one module only is used, whose inputs have thus to be properly matched

Moreover the back panel houses a Current Sum (Σ) output (on two bridged connectors) which generates a current proportional to the input signal multiplicity, i. e. to the number of channels over threshold, at a rate of -1.0 mA per hit (-50 mV per hit into a 50 Ω load) ± 20%. An OR output (with a Fan-Out of two) provides the logical OR of the output channels.

3.4. Setting the threshold and disabling the channels

For each channel of the N840-N841 the discriminator threshold is set via an 8 bit DAC. The threshold values can be programmed in a range from -1 mV to -255 mV with -1 mV steps. In order to set the threshold the Upper Switch (see § 2.5.2) must be placed on the THR position and the Lower Switch removed from the LCK position, then the channel that must be programmed is selected pulling up repeatedly the Lower Switch (the selected channel's Led lights up). Note that after the last channel, by pulling up the lower switch, the Leds ligth up all together and, at this point, the threshold setting is performed over all the channels (this value must be confirmed by placing the Lower Switch on the LCK position, otherwise it is ignored). The threshold value is set via the front panel Rotary handle (see § 2.5.3) and shown on the 4-Digit Display: 1 leads to a –1mV and 255 to a –255 mV threshold value; the step which follows 255 is four "*" appearing on the display (the relevant channel is inhibited), then again 0, 1, 2 etc.; inhibited channels' Leds are always lit when the lower switch is in lock (LCK) position. Once all the channels' thresholds have been set to the desired value the Lower Switch must be placed on the LCK (lower) position and the word *LOCK* appears on the display.

3.5. Setting the output pulse width

The output pulse width is adjustable on 8 bit from 5 to 40 ns and the chosen value is applied to a group of 8 channels each[2]. The Mod. N841 has two groups (Ch. 0, 1, 4, 5, 8, 9, 12, 13 and Ch. 2, 3, 6, 7, 10, 11, 14, 15, respectively), the Mod. N840 has only one group. The Upper Switch must be placed on the WDT position and the Lower Switch removed from the LCK position, then the group is selected pulling up repeatedly the Lower Switch (the selected group's Leds light up all together). The width's value is set via the Rotary Handle and shown on the display (0 leads to a 5 ns and 255 to a 40 ns width with a non-linear relation for intermediate values); the step which follows 255 is again 0, then 1, 2 etc. Once the Pulse Widths have been programmed the Lower Switch must be placed on the LCK position and the word *LOCK* appears on the display.

[2] Pulse duration ranges from 6 to 41 ns for negated outputs (/Out).