

# VFAT2 - Test procedures

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This document outlines the basic stages of setting up the chip for use, characterisation measurements procedures and operating procedures. It is intended to be used in conjunction with the VFAT2 operating manual.

## 1 The operation cycle

Figure 1 shows a flowchart of the operation cycle of VFAT2. This flow chart is also given in the operating manual and is repeated here because it outlines the sequence of commands for operating VFAT2.

A key point to the flowchart is direct entry into a “SLEEP” mode on applying power to the circuit. An internal power-on reset circuit generates a pulse that sets the internal programmable registers to default conditions. These default conditions mean that the chip is in a non-functional, minimum power consuming condition with only the I<sup>2</sup>C circuits remaining responsive. There are 2 other ways to enter SLEEP mode, these are application of a hard reset ”REh” or via I2C commands (SLEEPB bit : lsb of command register 0). The only active module in VFAT2 during SLEEP mode is

the I2C. Hence during this mode values can be written and read to and from the I2C registers. The values stored in the registers will not be applied to the circuit until the SLEEPB bit is set to ”1” and hence puts the chip into RUN mode. Once the SLEEPB

bit is set to ”1” the values written to the registers will be applied to the chip. Hence the DACs assume their programmed values and bias the analog part. Also the logic begins to run. At this stage the chip is consuming it’s RUN power. Since the I2C command is not a synchronous command the chip is not in a synchronised state. A

ReSync must be applied to the chip to start all counters (BCN and EN) and align

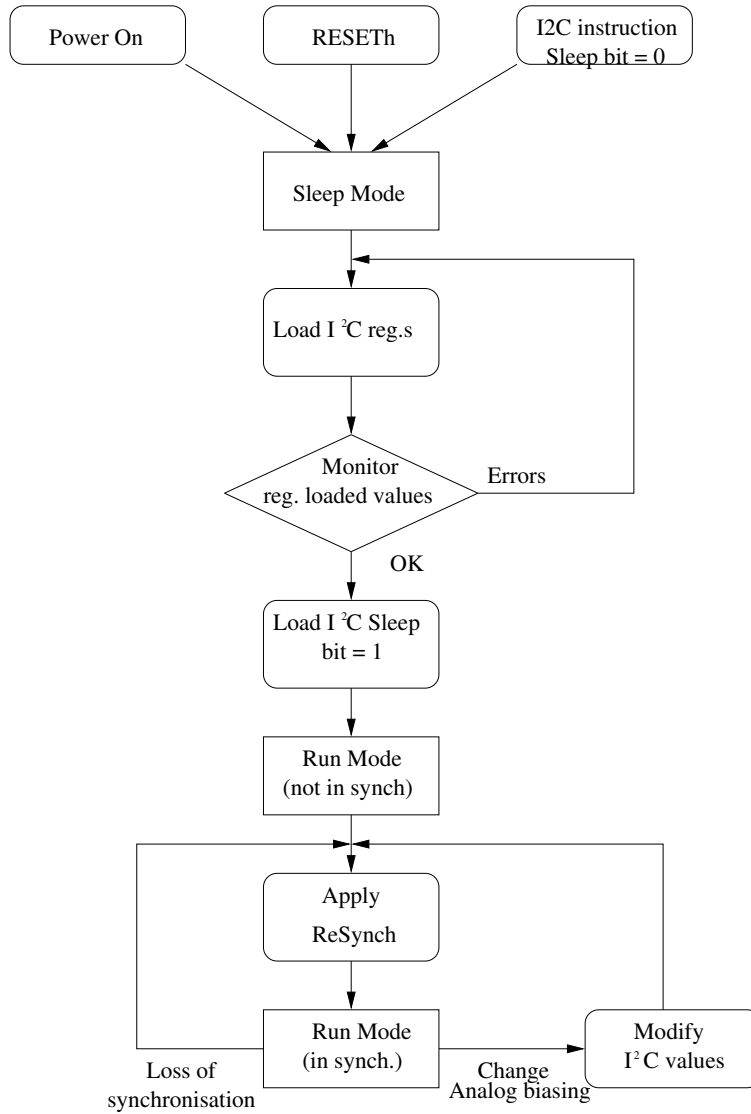


Figure 1: Flowchart of the operation cycle of VFAT2

the write pointers of SRAM1 to zero. ReSync is synchronous with the 40 MHz and is applied to all VFAT2s simultaneously hence synchronising the system. The chip is now in synchronised RUN mode and is capable of taking data. This is the mode it will stay during the data taking phase. If, for some reason or other such as SEU, a

chip loses sync., it may be resynchronised by the application of a ReSync command. The programmed values within the I2C registers may be modified with RUN mode.

However, it is recommended not to send I2C commands while data taking as it may degrade the signal to ratio of the chip. Also recommended is the application of a REs pulse immediately before a string of I2C commands especially after a long run of data taking and also to apply a ReSync after finishing the update of I2C commands. Entry

into the various test modes can be done at any stage.

## **2 Procedure for automated characterisation of VFAT2**

### **2.1 Power On**

The chip will enter SLEEP mode directly on application of power to the chip.

#### **2.1.1 Measure SLEEP power consumption**

A measurement of power consumption to the hybrid is made at this stage. During production testing a faulty chip drawing too much current could be identified as faulty and rejected immediately at this stage.

#### **2.1.2 Read ChipID**

Each chip has a unique identifier hardwired inside that may be read via I2C through principal registers 8 and 9. The identifier should be used to create a directory in which the measured results of this particular chip can be stored.

### **2.2 Write and Read to I2C registers**

Values may be written and then checked by reading back. Performing this function checks that the I2C is working correctly. Enter into RUN mode (SLEEPB=1).

### **2.3 Characterisation of the DACS**

The DAC response can be measure on a DAC by DAC basis through the DCU chip via the I2C.

The DACsel< 3 : 0 > bits of control register 1 determine which DAC to characterise. The DAC output is then routed to either DACoV or DACoI depending on whether the signal is a voltage or a current. These 2 VFAT2 outputs are connected to 2 DCU channels. Between VFAT2 and the DCU a potential divider exists on the board which divides the voltage by two and for the current an 8K ohm resistor to ground converts the output current to a voltage. The DCU chip contains an ADC which can be read by I2C. Hence to characterise a particular DAC the procedure of table 1 can be followed:

i)	Select a DAC via DACsel< 3 : 0 > ie. for IPreampln DACsel = 0001 .
ii)	Set IPreampln (principle register 2) too 0000 0000.
iii)	Take the measurement from the DCU
iv)	Repeat steps 2, and 3, incrementing by 1 up to 1111 1111.
v)	Store results and return DACsel to 0000 or pass to the next DAC.

Table 1: DAC Characterisation steps

The DAC "VCal" effects the amplitude of the calibration test pulse. VCal itself can be measured in the same way as previously described for the other DACs. To measure the absolute calibration amplitude however a slightly different procedure must be followed. First an understanding of how the calibration test pulse is constructed is necessary. The absolute amplitude of the calibration pulse is the difference between the 2 voltages "VHi" and "VLow". VHi is a baseline voltage generated with reference to a bandgap voltage inside the chip. VLow is controlled by VCal but is not exactly the same as VCal since there is a buffer in between the two voltages. The basic calibration circuit is shown in figure 2.

The calibration circuit generates a step between these VHi and VLow with a very fast rising edge and this pulse is delivered to the line CalOut. Each channel has a 100fF series capacitor connected to CalOut via a switch. Hence a selected channel will receive an injected charge to the pre-amp of approximately 0.1fC/mV.

Measuring this step in a dynamic way is impractical because the measurement would affect the pulse itself. Hence the measurement is made in dc, first on the baseline (VHi) then on VLow for all different possible values of VCal. Both measurements are made by taking the dc signal from CalOut.

Table 2 is the procedure to follow:

Having made this characterisation of the DAC currents, voltages and calibration inject pulse, lookup tables can be used such that the user can type in the bias voltage or current he desires or the charge he wishes to deliver to a particular channel.

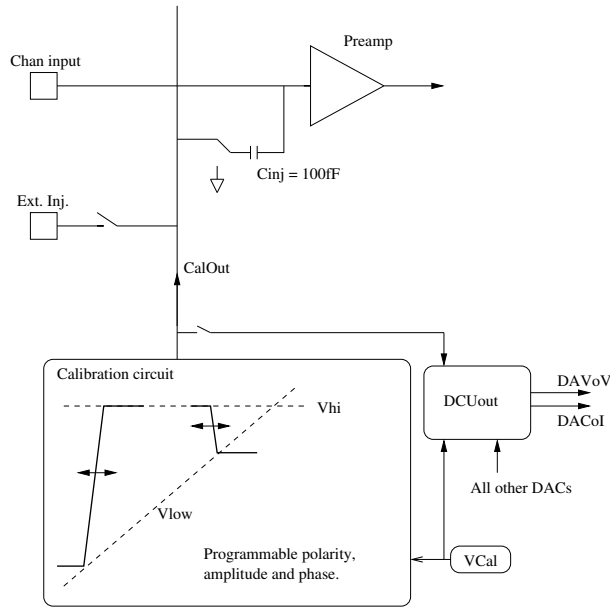


Figure 2: The Calibration pulse amplitude

i)	Select CalOut via DACsel< 3 : 0 > ie. DACsel = 1011 .
ii)	Route the baseline signal to CalOut in dc; set CalMode, 1 : 0 > to 10
iii)	Take a baseline measurement from the DCU
iv)	Set VCal (extended register 129) too 0000 0000.
v)	Take the measurement from the DCU
vi)	Repeat steps iv) and v) incrementing VCal by 1 up to 1111 1111.

Table 2: Characterise the calibration pulse

## 2.4 Measure power RUN mode

Change the "SLEEP" bit to 1 and then apply a ReSync pulse. The power can now be measured.

## 2.5 Pulse 1 channel - Set up Latency and verify data packet

The internal calibration pulse can be used for this procedure. The idea is to select one channel and regularly send a test pulse to that channel. By looking at the data packet the latency can be adjusted until the data packet gives a "1" on the channel injected. The the phase of the CalPulse can be adjusted to avoid uncertainties on timing. The procedure can be done in many ways but table 3 is an example:

Once the timing stabilities are settled the data packet can be checked.

i)	Select channel to inject charge ie. for channel 8 set extended register 8 to 0100 0000
ii)	Apply a large charge by setting VCal to correspond to say 8fC as given by the DAC characterisation stage and set the threshold voltage to a values below this. Simulation results can help to suggest starting values.
iii)	Set the board latency between the CalPulse and the LV1 pulse.
iv)	Set the VFAT2 latency (ext reg. 0). The value will be close to the board value but may not be exactly the same. The default VFAT2 value is 1000 0000 (3.2us).
v)	Apply the CalPulse and LV1 signals with a regular frequency (say 1 KHz or one CalPulse + LV1A every 1ms). Note : VFAT2 can handle up to 100KHz triggers
vi)	If instabilities in timing exist, ie. the signal is falling sometimes into one time slot or the neighbouring time slot the the phase of the CalPulse can be adjusted by setting CalPhase (extended register 132). The stability should be checked for different amplitudes of injected charge and CalPhase adjusted accordingly since the time walk of the comparator may cause timing instabilities.

Table 3: Pulse one channel

## 2.6 Logic Probe test

The logic circuits have been made such that internal signals can be monitored by the use of "Probe" pads. These probe pads are normally turned off but can be activated by setting high bit 4 of control reg. 1.

If VFAT2 is into the previous "Pulse 1 channel" mode then the internal logic signals can be viewed.

## 2.7 Check for dead channels

Here a CalPulse + LV1A should be sent one after another, changing the channel number of which to pulse each time (CalChan bit of each channel register). This will identify any channels that are not responding.

## 2.8 Adjusting Threshold and TrimDAC settings

There are two 8 bit DACs used for adjusting the main threshold. These are VT1 and VT2 (extended registers 130 and 131). In addition to this there is a 5 bit TrimDAC per channel adjustable by programming bits 4:0 of the 128 channel registers. There is also a 3 bit TrimDAC range setting in control register 3. Trimming of these DACs can be performed in the way described in table 4 :

## 2.9 S curve, noise measurements

The S curve is a histogram hits whilst varying the injected charge for a given threshold.

i)	For a given threshold two histograms can be made of measured thresholds for all channels, one with all TrimDAC settings = 00000 and the other with TrimDAC settings 11111.
ii)	If these histograms are well separated, the TrimDAC range should be adjusted so that the two histograms overlap by a small amount.
iii)	On a channel by channel basis; the TrimDAC should be adjusted to the midpoint between the two overlapping histograms.

Table 4: Trimming of thresholds

Measurements are taken for a given threshold ie 1fC. The signal is then ramped up from  $VCAL = 0000\ 0000$  to high levels of VCal. Many samples should be taken for each setting of VCAL. The resulting histogram will have the form of an S-curve, see figure 3.

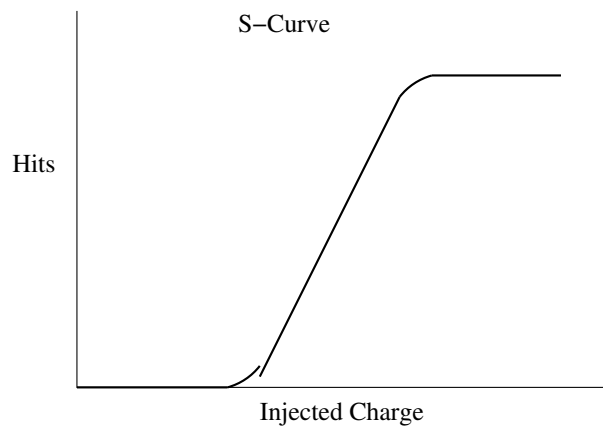


Figure 3: The S-curve

This curve should be measured for different threshold values. From this family of S-curves many analog characteristics can be deduced such as Noise, Threshold Value, Dynamic range and Linearity.

## 2.10 Minimum threshold

With zero charge injected the main threshold should be lowered until noise hits begin to appear. The minimum value of threshold for which noise hits do not appear is considered the minimum threshold for that particular channel. This measurement should be done on all channels and the overall minimum threshold should be given as a mean value with distribution.

## 2.11 Multiple Triggers, FULL flags etc.

In CMS consecutive triggers are forbidden. However triggers can occur every third clock cycle. The chip should be sent a stream of triggers with different intervals going

down to intervals of 3 clock periods and the data packets checked.

The chip can accommodate 128 simultaneously stored triggers. When SRAM2 contains 127 stored triggers the AFULL flag is raised in the data packet. When 128 triggers are stored the FULL flag is raised in the data packet. Further triggers will not be accepted by VFAT2 however it will count them and increment the EN. Data will continue to be read out of VFAT2 freeing up some space in SRAM2. When space becomes available new triggers will be accepted and their EN should be conserved.

## **2.12 Maximum trigger rate**

In CMS the maximum trigger rate follows a 100KHz Poisson distribution. VFAT2 is designed to run comfortably at this rate. It should however be checked. A 100KHz Poisson LV1A should be generated and then the data packets monitored to see if and when a full flag is raised.