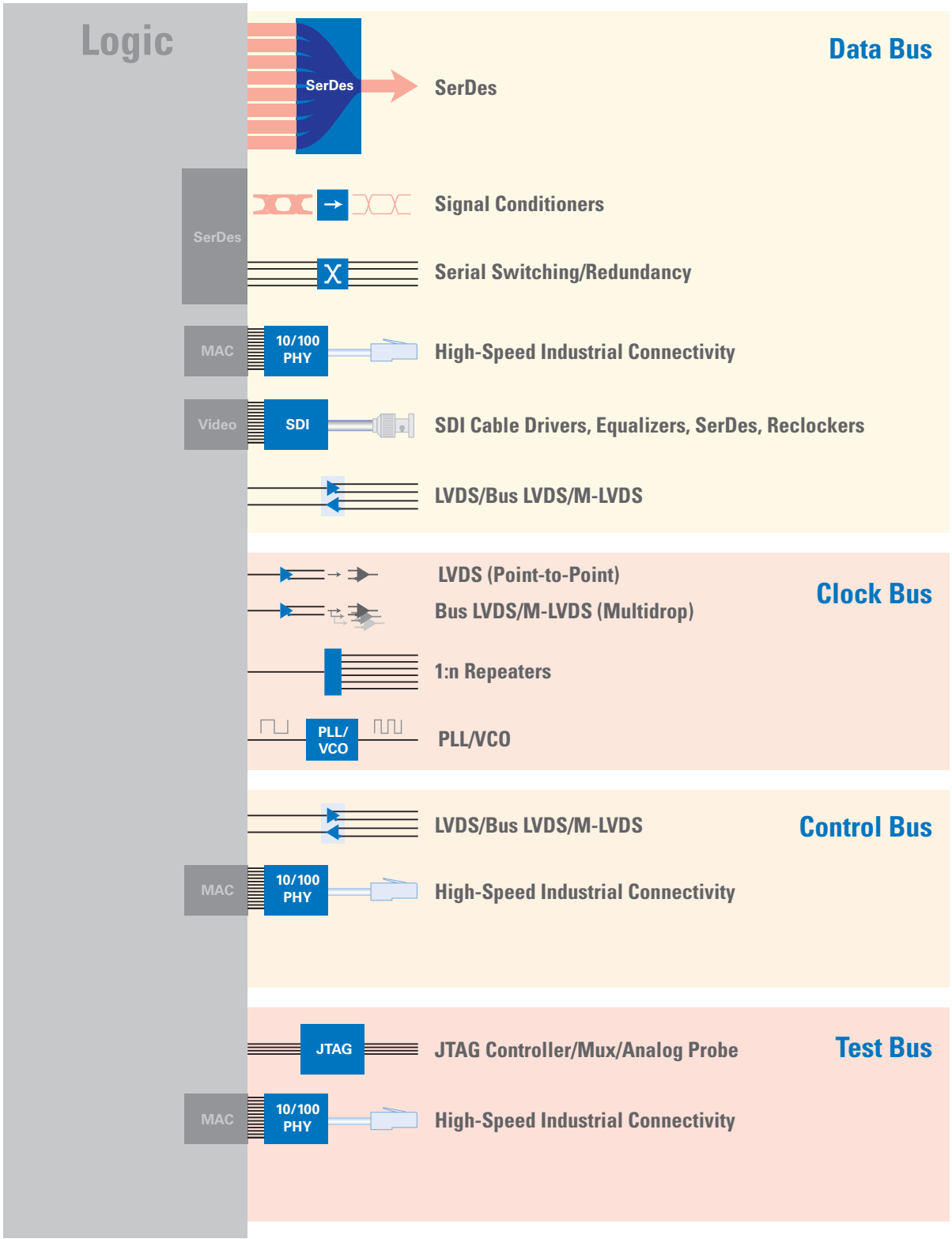
Interface Selection Guide

March 2007

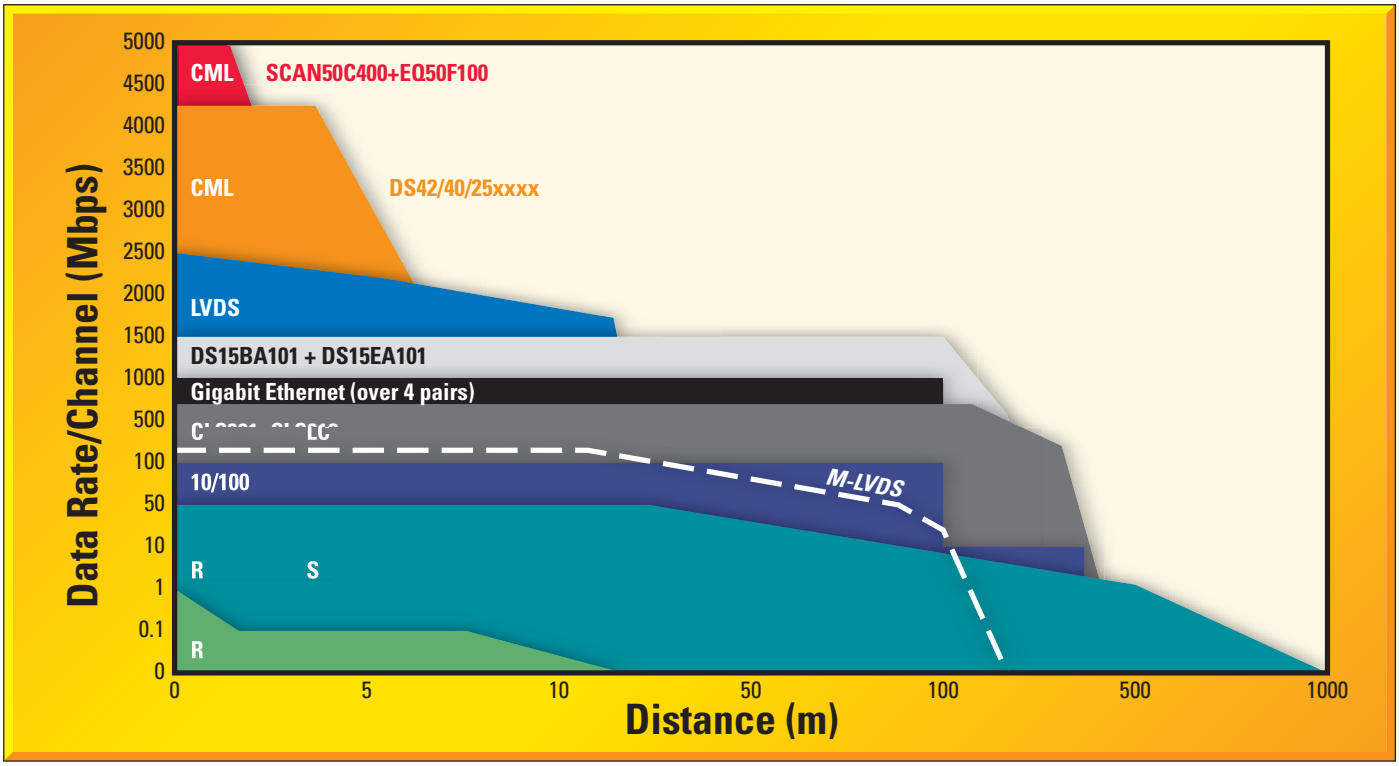
National Semiconductor

The Sight & Sound of Information

Product Overview



Interface Product Portfolio



	RS-422	RS-485	LVDS	Bus LVDS	M-LVDS	PECL	LVPECL	CML-3.3	CML-1.8
	TIA/EIA-422-B	TIA/EIA-485-A	TIA/EIA-644-A	—	TIA/EIA-899	—	—	—	—
	10 Mbps	10 Mbps	2.5 Gbps	2 Gbps	200 Mbps	10 Gbps	10 Gbps	10 Gbps	10 Gbps
	PP, MD	PP, MD, MP	PP	PP, MD, MP	PP, MD, MP	PP, MD, MP	PP, MD, MP	PP	PP
Voltage						Levels vary by vendor	Levels vary by vendor	Levels vary by vendor	Levels vary by vendor

10, 5, 4.5, 4, 3.5, 3, 2.5, 2, 1.5, 1, 0.5, 0, -10

Typical Transmitter Output Swing

Receiver Threshold

Receiver Input Voltage Range

PP = Point-to-Point
MD = Multidrop
MP = Multipoint

LVDS PHYs
Single-Ended to Differential

Single-Ended to Differential LVDS PHY Overview

Drivers

Single:	DS90LV011A (SOT23-5, LLP-8) DS90LV017A
Dual:	DS90LV027A DS90C401 (5V)
Quad:	DS90LV047A DS90C031 (5V)

Receivers

Single:	DS90LV012A (SOT23-5, LLP-8) DS90LV018A
Dual:	DS90LV028A DS90C402 (5V)
Quad:	DS90LV048A DS90C032 (5V)

Transceivers

Single:	DS90LV019 (LVDS) DS92LV010A (Bus LVDS) DS91C176/D176 (M-LVDS)
Quad:	DS92LV040A
9-Ch:	DS92LV090A SCAN92LV090 (JTAG)

1:6 Repeater

DS92CK16 (LVTTL to LVTTL or LVDS to LVTTL)

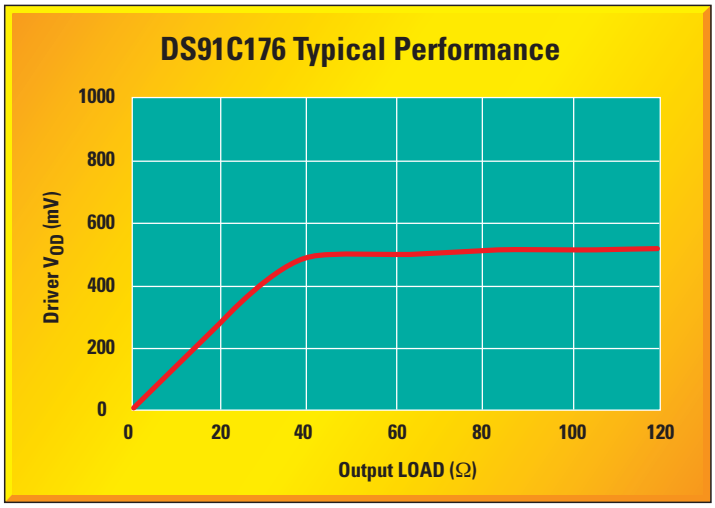
Drivers and Receivers

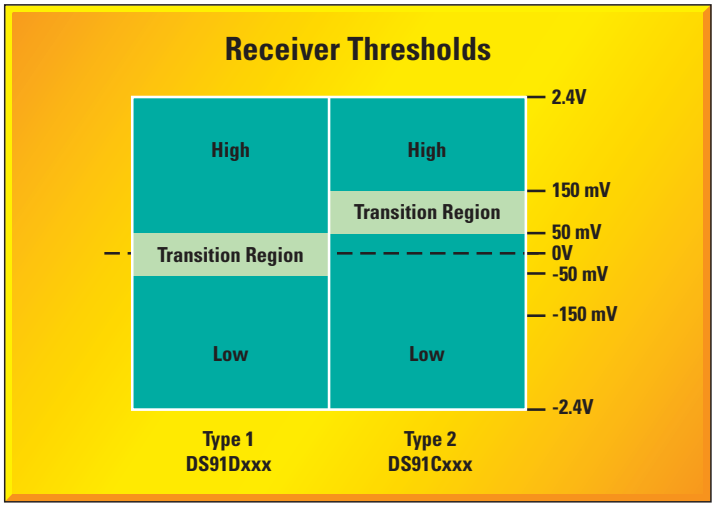
Single:	DS91C180/D180 (M-LVDS)
Dual:	DS90LV049 DS36C200 (5V)

Output Drive

- Bus LVDS
- M-LVDS

M-LVDS Multipoint Transceivers





Description

M-LVDS is a multipoint version of LVDS as described in the TIA/EIA-899 standard. M-LVDS is optimized for multipoint including features critical to multipoint applications such as:

- Controlled edge rates
- Higher drive
- Extended common mode
- Tighter receiver thresholds

Features

- 2 ns typical edge rates to minimize reflections
- Constant Output Voltage (Vod) for loads between 30 and 100Ω provides better noise margin even when driving heavy loads
- Common mode extended to -1.4 to 3.8V for improved noise immunity
- Tight 50 mV receiver thresholds add to noise margin
- Available with type 1 and type 2 (failsafe) receiver thresholds

The M-LVDS standard includes 2 types of receiver thresholds. Type 1 is a conventional LVDS input centered at 0V differential. Type 2 receivers have a built-in failsafe where the receiver threshold is offset by 100 mV. Zero volts on the receiver thresholds will always result in a logic LOW. In addition to providing a failsafe, type 2 receivers can be used in Wired-Or logic.

LVDS PHYs

Single-Ended to Differential

Product ID	Drivers	Receivers	LVDS Type	Max Speed/Ch (Mbps)	Supply Voltage	Temperature	Packaging	Comments
Transceivers								
New DS91C176TM	1	1	M-LVDS	100 MHz	3.3	-40 to +85°C	SOIC-8	M-LVDS, half duplex, type 2
New DS91D176TM	1	1	M-LVDS	100 MHz	3.3	-40 to +85°C	SOIC-8	M-LVDS, half duplex, type 1
New DS91C180TM	1	1	M-LVDS	100 MHz	3.3	-40 to +85°C	SOIC-14	M-LVDS, full duplex, type 2
New DS91D180TM	1	1	M-LVDS	100 MHz	3.3	-40 to +85°C	SOIC-14	M-LVDS, full duplex, type 1
DS90LV019TM/TMTC	1	1	LVDS	155	3.3 or 5	-40 to +85°C	SOIC-14, TSSOP-14	
DS92LV010ATM	1	1	Bus LVDS	155	3.3 or 5	-40 to +85°C	SOIC-8	3.3V or 5V operation
DS92LV040ATLQA	4	4	Bus LVDS	200	3.3	-40 to +85°C	LLP-44	Edge rate ctrl, low skew
DS92LV090ATVEH	9	9	Bus LVDS	200	2.7 - 3.6	-40 to +85°C	PQFP-64	Low part-to-part skew
SCAN92LV090SLC/TVEH	9	9	Bus LVDS	200	2.7 - 3.6	-40 to +85°C	BGA-64, PQFP-64	Small footprint, JTAG
Single Drivers and Receivers								
DS90LV011ATMF	1	0	LVDS	400	3.3	-40 to +85°C	SOT23-5	Tiny package
DS90LV011AHMF AECQ-100	1	0	LVDS	400	3.3	-40 to +125°C	SOT23-5	Extreme temperature range
DS90LV012ATMF	0	1	LVDS	400	3.3	-40 to +85°C	SOT23-5	Tiny package
DS90LT012ATMF	0	1	LVDS	400	3.3	-40 to +85°C	SOT23-5	Integrated termination
DS90LT012AHMF AECQ-100	0	1	LVDS	400	3.3	-40 to +125°C	SOT23-5	Extreme temperature range
DS90LV017ATM[2]	1	0	LVDS	400	3.3	-40 to +85°C	SOIC-8	
DS90LV018ATM[2]	0	1	LVDS	400	3.3	-40 to +85°C	SOIC-8	
Dual Drivers and Receivers								
DS90C401M	2	0	LVDS	155	5	0 to +70°C	SOIC-8	
DS90C402M	0	2	LVDS	155	5	0 to +70°C	SOIC-8	
DS36C200M	2	2	LVDS	155	5	0 to +70°C	SOIC-14	1394 link
DS90LV027ATM[2]	2	0	LVDS	400	3.3	-40 to +85°C	SOIC-8	
DS90LV027AHM AECQ-100	2	0	LVDS	400	3.3	-40 to +125°C	SOIC-8	Extreme temperature range
DS90LV028ATM/ATLD[2]	0	2	LVDS	400	3.3	-40 to +85°C	SOIC-8, LLP-8	
DS90LV028AHM AECQ-100	0	2	LVDS	400	3.3	-40 to +125°C	SOIC-8	Extreme temperature range
DS90LV049TMT[2]	2	2	LVDS	400	3.3	-40 to +85°C	TSSOP-16	
DS90LV049HMT AECQ-100	2	2	LVDS	400	3.3	-40 to +125°C	TSSOP-16	Extreme temperature range
Quad Drivers and Receivers								
DS90C031BTM	4	0	LVDS	155	5	-40 to +85°C	SOIC-16	Power off hi-Z
DS90C032BTM	0	4	LVDS	155	5	-40 to +85°C	SOIC-16	Power off hi-Z
DS90C031E-QML[1]	4	0	LVDS	100	5	-55 to +125°C	LCC-20	Military-883
DS90C032E-QML[1]	0	4	LVDS	100	5	-55 to +125°C	LCC-20	Military-883
DS90C031W-QML[1]	4	0	LVDS	100	5	-55 to +125°C	Flatpack-16	Military-883
DS90C032W-QML[1]	0	4	LVDS	100	5	-55 to +125°C	Flatpack-16	Military-883
DS90LV031ATM/ATMTC	4	0	LVDS	400	3.3	-40 to +85°C	SOIC-16, TSSOP-16	
DS90LV031BTM[1,2]	4	0	LVDS	400	3.3	-40 to +85°C	SOIC-16	Undershoot protection
DS90LV032ATM/ATMTC[1,2]	0	4	LVDS	400	3.3	-40 to +85°C	SOIC-16, TSSOP-16	
DS90LV047ATM/ATMTC[2]	4	0	LVDS	400	3.3	-40 to +85°C	SOIC-16, TSSOP-16	
DS90LV048ATM/ATMTC[2]	0	4	LVDS	400	3.3	-40 to +85°C	SOIC-16, TSSOP-16	
1:n Repeaters								
DS92CK16TMTC	1	6	Bus LVDS	125 MHz	3.3	-40 to +85°C	TSSOP-24	Configurations: A) 1 LVTTL input to 6 LVTTL + 1 BLVDS outputs B) 1 LVDS to 6 LVTTL

[1] These products are also available qualified to QML for space and/or military applications
[2] Use evaluation board part number LVDS47/48EVK

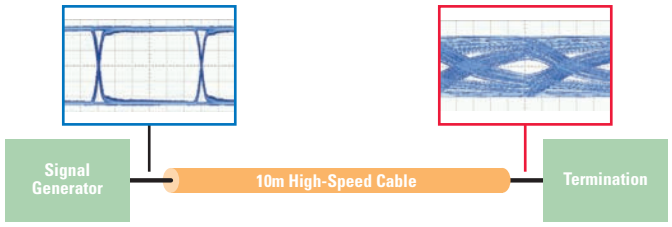
Pre-Emphasis/De-Emphasis

Signal conditioners boost FPGA/ASIC serial I/O signals to enable reliable transmission across lossy cables, backplanes, and FR4 traces. Pre-emphasis or de-emphasis pre-distorts the output signal to compensate for the filtering effects of the interconnect.

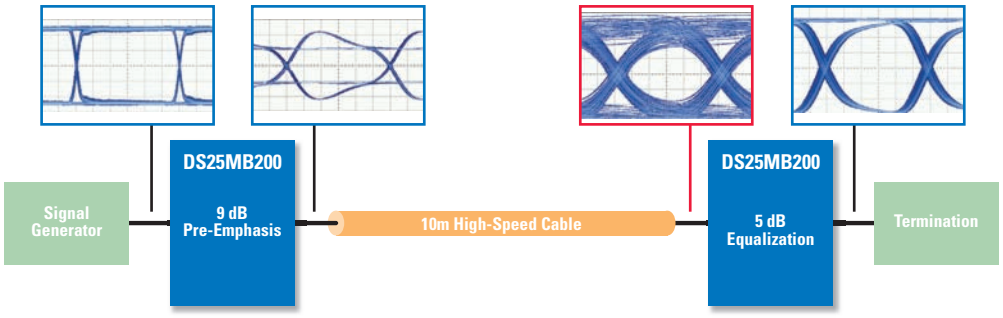
Equalization

Receive equalization applies a high pass filter to incoming signal to cancel out the low pass filter effect of the interconnect. This reduces the amplitude difference between the lower frequency and the higher frequency components of the bit stream.

10m High-Speed Cable
2.5 Gbps, PRBS-7

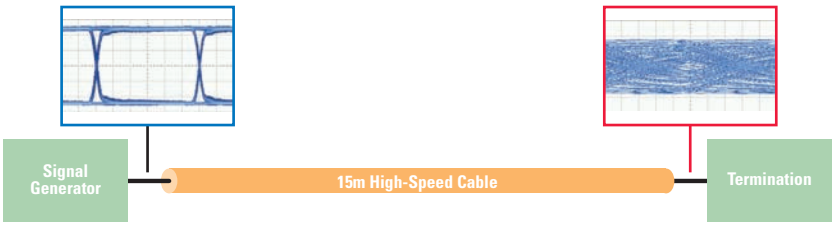


Eye pattern not acceptable after 10m high-speed cable

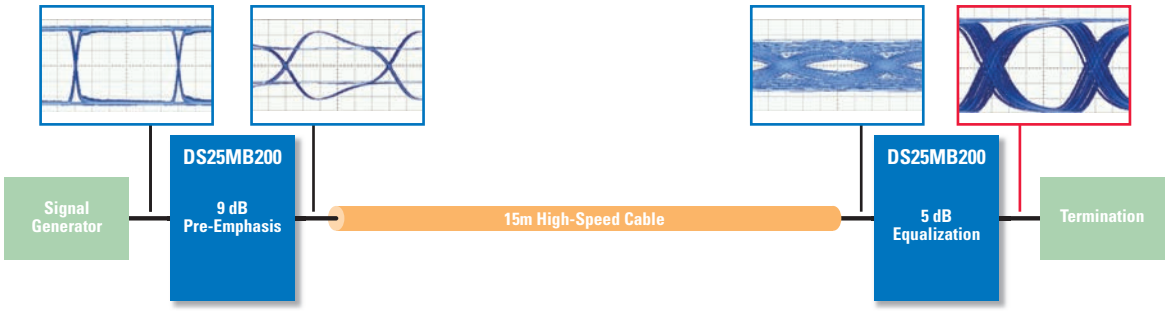


Eye pattern acceptable even with transmit de-emphasis only

15m High-Speed Cable
2.5 Gbps, PRBS-7



Eye pattern not acceptable after 15m high-speed cable



Eye pattern acceptable with transmit de-emphasis and receive equalization

LVDS and CML PHYs

Cable Extension and Switching/Redundancy

DS15BA101 + DS15EA101 – 1.5 Gbps Cable Extender Chipset

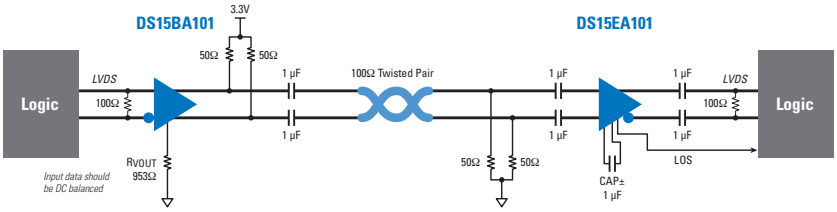
Description

The DS15BA101 cable driver and DS15EA101 equalizer provide a lower cost, more flexible alternative to fiber for twisted pair and coaxial cables up to hundreds of meters.

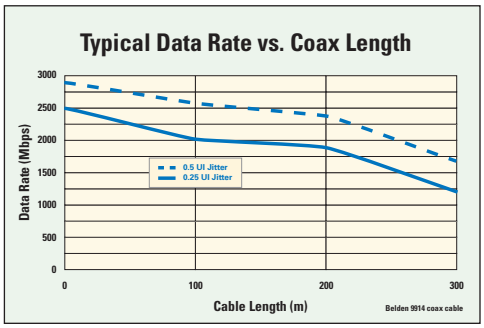
A complete evaluation kit reference design is available.

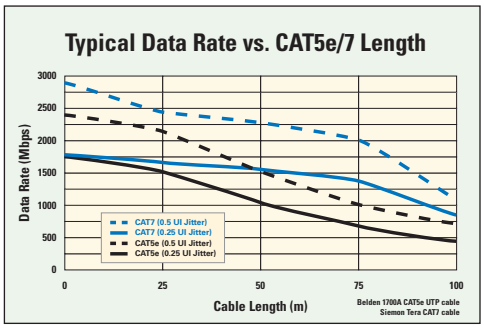
Features

- ½ the cost of optical solutions
- Easy installation and maintenance
- Data rates up to 1500 Mbps
- Drive up to 300m copper cable
- Supports CATx twisted pair and coaxial cables
- Fully adaptive, easy-to-use
- Test reports available
- Evaluation boards reference design order number: DriveCable02EVK

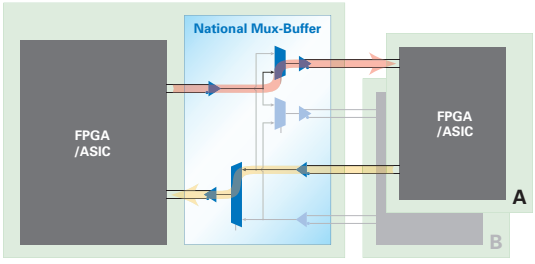


CAT5e twisted pair cable application example





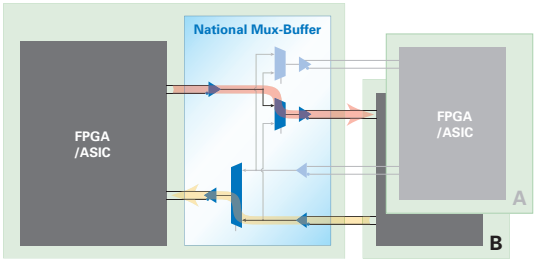
Redundancy/Switching – Using a DSxxMBx00 Mux-Buffer Device



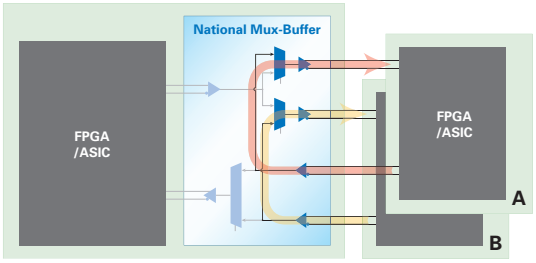
Normal operation

Features

- Integrates 1:1 redundancy function
- Single and dual channel integrated 2:1/1:2 multiplexer/buffer devices available
- LVDS up to 2 Gbps and CML versions up to 4.25 Gbps
- Signal conditioning pre-emphasis/de-emphasis and receive equalization on chip
- Integrated termination saves board area, improves signal quality
- Also available 2 x 2 and 4 x 4 crosspoint switches as well as 1:10 repeaters for other switching/redundancy applications



Failover operation



Loop back operation (available on selected devices)

LVDS and CML PHYs
Differential to Differential

Differential to Differential PHY Overview

Buffers

Single: DS25BR100 (3.125 Gbps, LVDS)
DS90LV001 (800 Mbps, LVDS)
DS92001 (Bus LVDS)
DS15BA101 (LVPECL)
DS15EA101 (Cable EQ)
EQ50F100 (Equalizer)

Dual: DS92LV222A (dual buffer or single 1:2 repeater)

Quad: DS15BR400 (1500 Mbps, termination)
DS15BR401 (1500 Mbps)
SCAN90004 (JTAG)

Quad Transceiver:
DS25BR400 (2500 Mbps, CML)
DS42BR400 (4250 Mbps, CML)

Crosspoint Switches

2 x 2: DS90CP22 (800 Mbps)
SCAN90CP02 (1500 Mbps)

4 x 4: DS90CP04 (2500 Mbps)

Multiplexers

Single 1:2: DS92LV222A (200 Mbps)

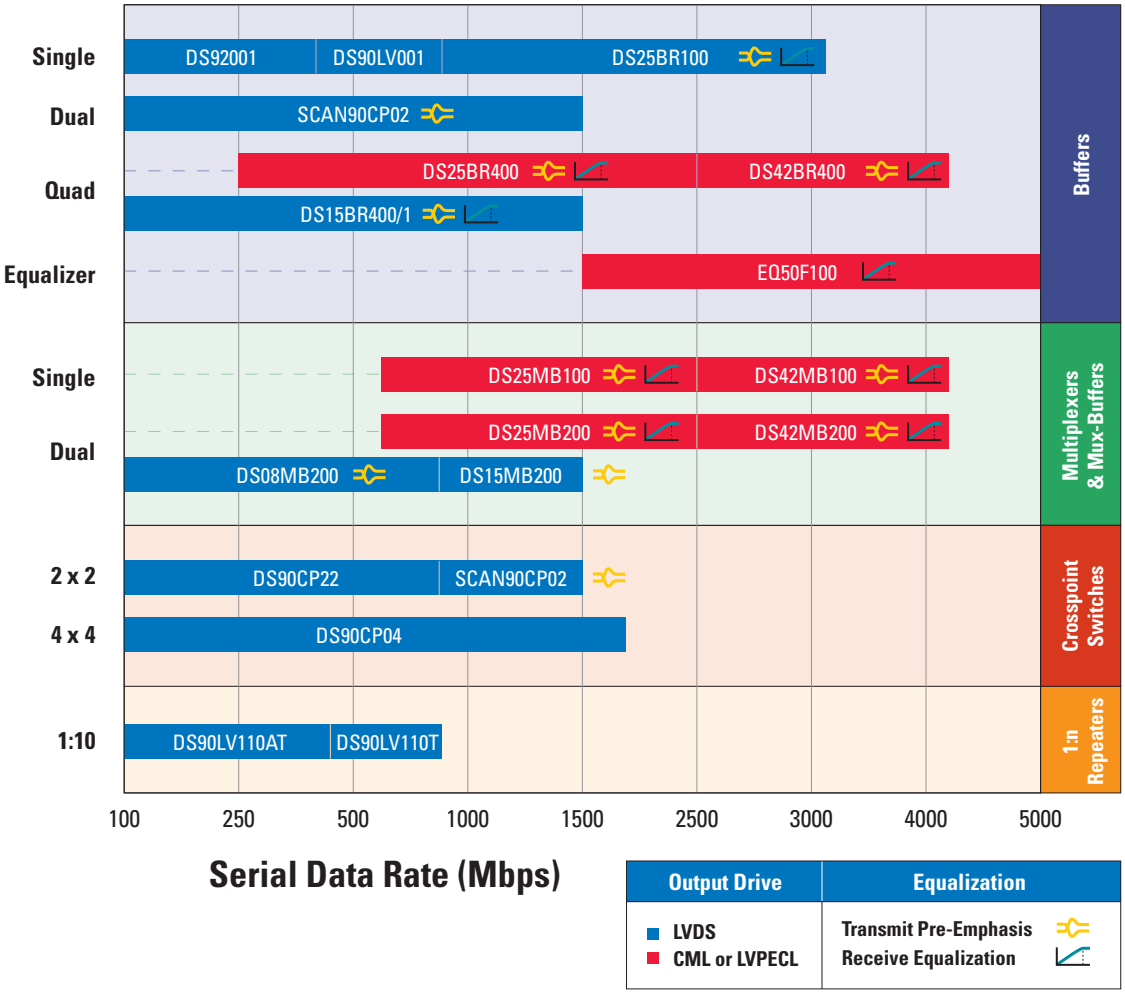
Single 1:2/2:1
DS25MB100 (2500 Mbps, CML)
DS42MB100 (4250 Mbps, CML)

Dual 1:2/2:1:
DS15MB200 (1500 Mbps)
SCAN15MB200 (1500 Mbps, JTAG)
DS25MB200 (2500 Mbps, CML)
DS40MB200 (4000 Mbps, CML)
DS42MB200 (4250 Mbps, CML)

1:10 Repeater

DS90LV110T/AT (800/400 Mbps)

Output Drive	Equalization
Bus LVDS CML or LVPECL	Transmit Pre-Emphasis/De-Emphasis Receive Equalization



Output Drive	Equalization
LVDS CML or LVPECL	Transmit Pre-Emphasis Receive Equalization

LVDS and CML PHYs
Differential to Differential

Product ID	Function	In-puts	Out-puts	Switching/Redundancy: Muxing Options	Input Compatibility	Output	Signal Conditioning: Pre-emphasis (dB)[1]	Signal Conditioning: Receive Equal-ization (dB)	Max Speed/ Ch (Mbps)	Packaging	Comments
Buffers											
DS90LV001TM/TLD	Single LVDS buffer	1	1	—	LVDS/LVPECL/CML	LVDS	—	—	800	SOIC/LLP-8	
DS92001TMA/TLD	Single bus LVDS buffer	1	1	—	LVDS/LVPECL/CML	Bus LVDS	—	—	400	SOIC/LLP-8	
New DS15BA101SD	Adjustable output buffer	1	1	—	LVDS/LVPECL/CML	LVPECL	—	—	1500	LLP-8	Adjustable output swing
New DS15EA101SQ	Adaptive cable equalizer	1	1	—	LVPECL	CML	—	Adaptive	1500	LLP-16	Use with DS15BA101
New DS25BR100TSD	Single LVDS buffer	1	1	—	LVDS/LVPECL/CML	LVDS	0/6	3/6	3125	LLP-8	Int termination, 8 kV ESD
EQ50F100LR	Fixed receive equalizer	1	1	—	LVDS/LVPECL/CML	CML	—	20	6250	LLP-6	For backplanes or cable
DS92LV222ATM	Dual repeater/mux	2	2	2:2, 1:2	LVDS/LVPECL/CML	Bus LVDS	—	—	155	SOIC-16	Repeater, mux, 1:2 modes
DS90LV804TSQ	Quad LVDS buffer	4	4	—	LVDS/LVPECL/CML	LVDS	—	—	800	LLP-32	Int termination, 15 kV ESD
DS90LV004TVS	Quad LVDS buffer	4	4	—	LVDS/LVPECL/CML	LVDS	0/2/4/6	—	1500	TQFP-48	Int termination, 15 kV ESD
DS15BR400TSQ/TVS	Quad LVDS buffer	4	4	—	LVDS/LVPECL/CML	LVDS	0/6	—	2000	LLP-32, TQFP-48	Int termination, 15 kV ESD
DS15BR401TSQ/TVS	Quad LVDS buffer	4	4	—	LVDS/LVPECL/CML	LVDS	0/6	—	2000	LLP-32, TQFP-48	15 kV ESD
SCAN90004TVS	Quad LVDS buffer	4	4	—	LVDS/LVPECL/CML	LVDS	0/2/4/6	—	1500	TQFP-48	Int termination, JTAG
DS25BR400TSQ	Quad CML buffer	8	8	Loopback	LVDS/LVPECL/CML	CML	0/-3/-6/-9	0/5	2500	LLP-60	Int termination, 6 kV ESD
DS42BR400TSQ	Quad CML buffer	8	8	Loopback	LVDS/LVPECL/CML	CML	0/-3/-6/-9	0/5	4250	LLP-60	Int termination, 6 kV ESD
Multiplexers and Mux-Buffers											
New DS25MB100TSQ	2:1/1:2 mux/buffer	3	3	2:1/1:2, LB	LVDS/LVPECL/CML	CML	0/-3/-6/-9	0/5	2500	LLP-36	Int termination, 6 kV ESD
New DS42MB100TSQ	2:1/1:2 mux/buffer	3	3	2:1/1:2, LB	LVDS/LVPECL/CML	CML	0/-3/-6/-9	0/5	4250	LLP-36	Int termination, 6 kV ESD
DS08MB200TSQ	Dual 2:1/1:2 mux/buffer	6	6	2:1/1:2	LVDS/LVPECL/CML	LVDS	—	—	800	LLP-48	15 kV ESD
DS15MB200TSQ	Dual 2:1/1:2 mux/buffer	6	6	2:1/1:2	LVDS/LVPECL/CML	LVDS	0/6	—	1500	LLP-48	15 kV ESD
SCAN15MB200TSQ	Dual 2:1/1:2 mux/buffer	6	6	2:1/1:2	LVDS/LVPECL/CML	LVDS	0/6	—	1500	LLP-48	JTAG
DS25MB200TSQ	Dual 2:1/1:2 mux/buffer	6	6	2:1/1:2, LB	LVDS/LVPECL/CML	CML	0/-3/-6/-9	0/5	2500	LLP-48	Int termination, 6 kV ESD
DS40MB200SQ	Dual 2:1/1:2 mux/buffer	6	6	2:1/1:2, LB	LVDS/LVPECL/CML	CML	0/-3/-6/-9	0/5	4000	LLP-48	Int termination, 6 kV ESD
DS42MB200TSQ	Dual 2:1/1:2 mux/buffer	6	6	2:1/1:2, LB	LVDS/LVPECL/CML	CML	0/-3/-6/-9	0/5	4250	LLP-48	Int termination, 6 kV ESD
Crosspoint Switches											
SCAN90CP02SP/VY	2 x 2 crosspoint	2	2	2 x 2	LVDS/LVPECL/CML	LVDS	0/2/3.5/5	—	1500	LLP-28, LQFP-32	JTAG, 1149.6
DS90CP22M-8/MT	2 x 2 crosspoint	2	2	2 x 2	LVDS/LVPECL/CML	LVDS	—	—	800	TSSOP-16, SOIC-16	
DS90CP04TLD	4 x 4 crosspoint	4	4	4 x 4	LVDS/LVPECL/CML	LVDS	—	—	2500	LLP-32	Small footprint
1:n Repeaters											
DS90LV110ATMT	1:10 LVDS repeater	1	10	1:10	LVDS/LVPECL/CML	LVDS	—	—	400	TSSOP-28	Input failsafe

LB = Loopback [1]CML devices in this column that feature de-emphasis show a negative dB

SerDes

Selecting the Right SerDes

SerDes

Embedded Clock

10:1	DS92LV1021/1212 (16 to 40 MHz) DS92LV1023/1224 (40 to 66 MHz) SCAN921023/1224 (20 to 66 MHz) SCAN921025/1226H (20 to 80 MHz) SCAN928028/6260 (Multi-Channel)
16:1	DS92LV16 (25 to 80 MHz)
18:1	DS92LV18 (15 to 66 MHz) SCAN921821 (Dual Tx, 15 to 66 MHz)
24:1	DS90C241/124 (5 to 35 MHz) DCB DS90UR241/124 (5 to 43 MHz) DCB

Channel Link Parallel Clock

21:3	DS90CR213/214 (5V, 20 to 66 MHz) DS90CR215/216A (3.3V, 20 to 66 MHz) DS90CR217/218A (3.3V, 20 to 85 MHz)
28:4	DS90CR283/284 (5V, 20 to 66 MHz) DS90CR285/286A (3.3V, 20 to 66 MHz) DS90CR287/288A (3.3V, 20 to 85 MHz)
48:8	DS90CR481/482 (65 to 112 MHz) DCB DS90CR483/484 (33 to 112 MHz) DCB DS90CR485/486 (66 to 133 MHz) DCB

4:1 Bit Interleave

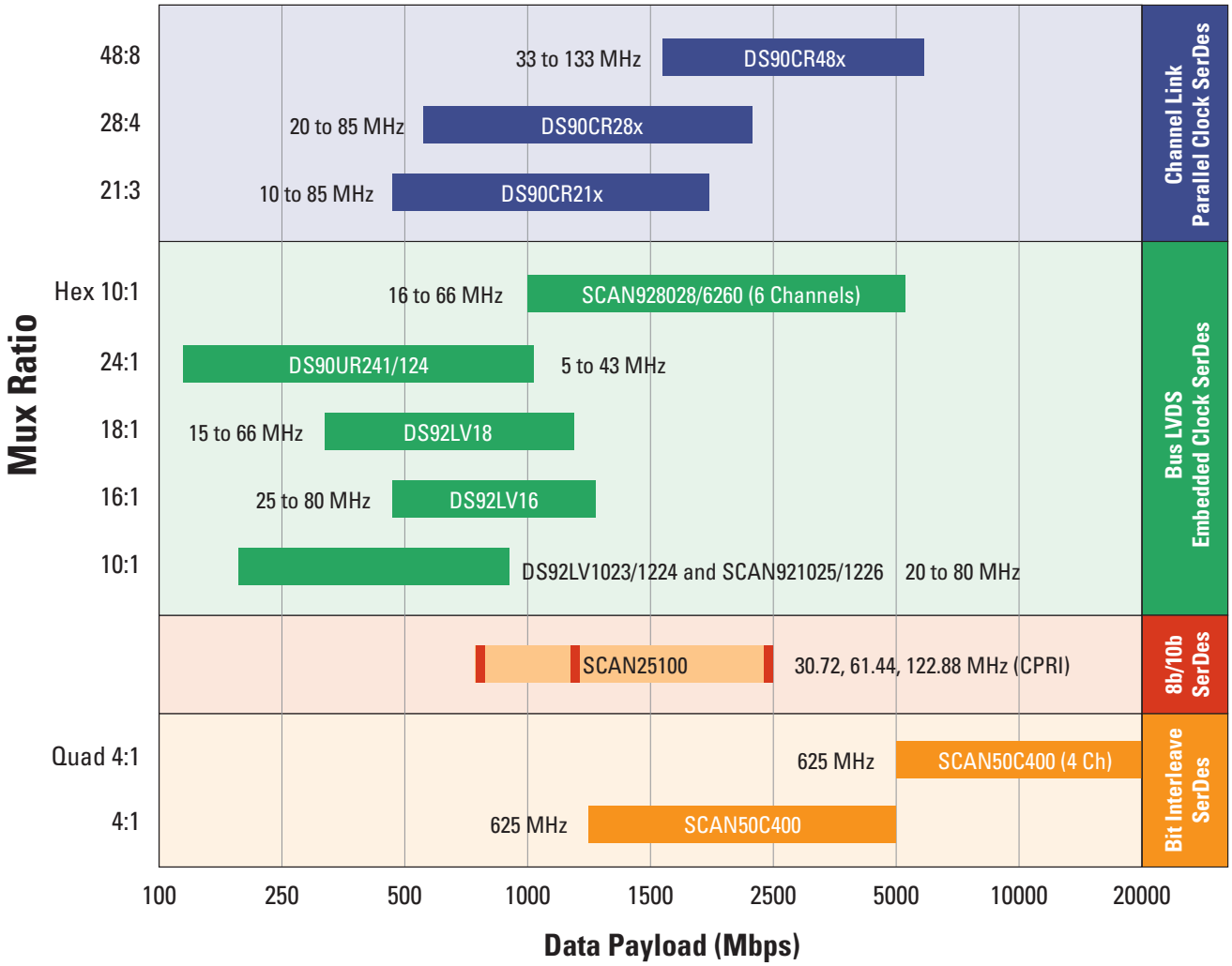
SCAN50C400 (Quad 5 Gbps)

8b/10b CPRI SerDes

SCAN25100/12100 DCB

Equalization

Transmit Pre-Emphasis	
Receive Equalization	
DC Balance	DCB



SerDes

Channel Link Parallel Clock SerDes Products

Product ID	Mux Ratio	Function	Bus Speed (MHz)	Max Throughput (Gbps)	Supply Voltage	Temperature	Packaging	Eval Kit
21-bit								
DS90CR213MTD	21:3	Transmitter	20 to 66	1.38	5	-10 to +70°C	TSSOP-48	See Note 1
DS90CR214MTD	21:3	Receiver	20 to 66	1.38	5	-10 to +70°C	TSSOP-48	See Note 1
DS90CR215MTD	21:3	Transmitter	10 to 66	1.38	3.3	-40 to +85°C	TSSOP-48	See Note 1
DS90CR216AMTD	21:3	Receiver	20 to 66	1.38	3.3	-40 to +85°C	TSSOP-48	See Note 1
DS90CR217MTD	21:3	Transmitter	20 to 85	1.78	3.3	-10 to +70°C	TSSOP-48	See Note 1
DS90CR218AMTD	21:3	Receiver	12 to 85	1.78	3.3	-10 to +70°C	TSSOP-48	See Note 1
28-bit								
DS90CR283MTD	28:4	Transmitter	20 to 66	1.84	5	-10 to +70°C	TSSOP-56	See Note 1
DS90CR284MTD	28:4	Receiver	20 to 66	1.84	5	-10 to +70°C	TSSOP-56	See Note 1
DS90CR285MTD	28:4	Transmitter	20 to 66	1.84	3.3	-40 to +85°C	TSSOP-56	See Note 1
DS90CR286AMTD	28:4	Receiver	20 to 66	1.84	3.3	-40 to +85°C	TSSOP-56	See Note 1
DS90CR287MTD	28:4	Transmitter	20 to 85	2.38	3.3	-10 to +70°C	TSSOP-56	CLINK3V28BT-85
DS90CR288AMTD	28:4	Receiver	20 to 85	2.38	3.3	-10 to +70°C	TSSOP-56	CLINK3V28BT-85
48-bit (with DC Balance and Pre-Emphasis)								
DS90CR481VJD	48:8	Transmitter	65 to 112	5.37	3.3	-10 to +70°C	TQFP-100	CLINK3V48BT-112
DS90CR482VS[2]	48:8	Receiver	65 to 112	5.37	3.3	-10 to +70°C	TQFP-100	CLINK3V48BT-112
DS90CR483VJD	48:8	Transmitter	33 to 112	5.37	3.3	-10 to +70°C	TQFP-100	CLINK3V48BT-112
DS90CR484VJD	48:8	Receiver	33 to 112	5.37	3.3	-10 to +70°C	TQFP-100	CLINK3V48BT-112
DS90CR485VS[2]	48:8	Transmitter	66 to 133	6.38	2.5/3.3	-10 to +70°C	TQFP-100	CLINK3V48BT-133
DS90CR486VS[2]	48:8	Receiver	66 to 133	6.38	3.3	-10 to +70°C	TQFP-100	CLINK3V48BT-133

[1] Use 85 MHz 28-bit evaluation kit for proof of concept. This evaluation kit can be reworked to accept non-85 MHz, non-28-bit devices if necessary.

[2] Package codes: National has recently moved to 2-letter package code suffixes. Therefore, the new VS code refers to the same TQFP-100 package as the old VJD code.

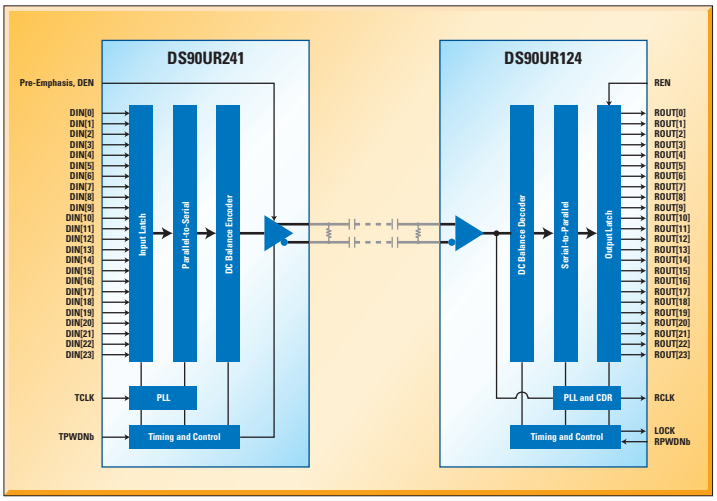
DS90UR241/124 – 5 to 43 MHz 24-bit Serializer/Deserializer with DC-Balance and Pre-Emphasis

Description

The DS90UR241/124 is a 24-bit serializer/deserializer chipset with automatic receiver lock to any data pattern for "plug and go" applications. DC-balance and programmable pre-emphasis drive long, AC-coupled cables including inexpensive CAT5 twisted pair. The DS90UR124 deserializer requires no external clock reference, reducing receiver board complexity and cost. The chipset is fully AEC-Q100 qualified for automotive and other extreme applications.

Features

- Serializes 24 bits at 5 to 43 MHz (125 to 1032 Mbps)
- Receiver automatically locks to any data pattern without external clock
- DC-balance encoding for AC-coupled and optical interconnects
- Drives 10m twisted pair cable
- At-speed BIST pattern generation/verification
- 10 kV ESD (ISO-10605) and hot plug protection
- Extreme -40 to +105°C temperature range



SerDes

Embedded Clock and Bit Interleave SerDes Products

Product ID	Mux Ratio	Function	#Ser	#Des	Clock Speed (MHz)	Max Rate/Ch (Mbps)	Max Throughput (Mbps)	Temperature	Packaging	Eval Kit
Single-Channel 10-bit SerDes										
DS92LV1021ATMSA	10:1	Serializer	1	—	16 to 40	400	400	-40 to +85°C	SSOP-28	BLVDS03
DS92LV1212AMSA	10:1	Deserializer	—	1	16 to 40	400	400	-40 to +85°C	SSOP-28	BLVDS03
DS92LV1023ETMSA	10:1	Serializer	1	—	30 to 66	660	660	-40 to +85°C	SSOP-28	BLVDS03
DS92LV1224TMSA	10:1	Deserializer	—	1	30 to 66	660	660	-40 to +85°C	SSOP-28	BLVDS03
SCAN921023SLC	10:1	Serializer	1	—	20 to 66	660	660	-40 to +85°C	BGA-49	BLVDS03
SCAN921224SLC	10:1	Deserializer	—	1	20 to 66	660	660	-40 to +85°C	BGA-49	BLVDS03
SCAN921025SLC	10:1	Serializer	1	—	30 to 80	800	800	-40 to +85°C	BGA-49	BLVDS03
SCAN921226SLC	10:1	Deserializer	—	1	30 to 80	800	800	-40 to +85°C	BGA-49	BLVDS03
SCAN921025HSM	10:1	Serializer	1	—	20 to 80	800	800	-40 to +125°C	BGA-49	BLVDS03
SCAN921226HSM	10:1	Deserializer	—	1	20 to 80	800	800	-40 to +125°C	BGA-49	BLVDS03
Multi-Channel 10-bit SerDes										
DS92LV1260UJB	10:1	Deserializers	—	6	20 to 40	400	2400	-40 to +85°C	LBGA-196	BLVDS03
SCAN921260UJB	10:1	Deserializers	—	6	20 to 66	660	3960	-40 to +85°C	LBGA-196	BLVDS03
SCAN926260TUF	10:1	Deserializers	—	6	16 to 66	660	3960	-40 to +85°C	LBGA-196	BLVDS03
DS92LV8028TUF	10:1	Serializers	8	—	25 to 66	660	5280	-40 to +85°C	LBGA-196	BLVDS03
SCAN928028TUF	10:1	Serializers	8	—	25 to 66	660	5280	-40 to +85°C	LBGA-196	BLVDS03
16-bit										
DS92LV16TVHG	16:1	SerDes	1	1	25 to 80	1280	1280 per direction	-40 to +85°C	PQFP-80	BLVDS16EVK
18-bit										
DS92LV18TVV	18:1	SerDes	1	1	15 - 66	1188	1188 per direction	-40 to +85°C	PQFP-80	LVDS-18B-EVK
SCAN921821TSM	18:1	Serializers	2	—	15 - 66	1188	1188 per direction	-40 to +85°C	FBGA-100	LVDS-18B-EVK
24-bit (with DC-Balance and Pre-Emphasis)										
New DS90C241 IVS AECQ-100	24:1	Serializer	1	—	5 - 35	840	840	-40 to +105°C	TQFP-48	SERDES24-35USB
New DS90C124 IVS AECQ-100	1:24	Deserializer	—	1	5 - 35	840	840	-40 to +105°C	TQFP-48	SERDES24-35USB
New DS90UR241 IVS AECQ-100	24:1	Serializer	1	—	5 - 43	1032	1032	-40 to +105°C	TQFP-48	SERDESUR-43USB SERDESUR-43SMA
New DS90UR124 IVS AECQ-100	1:24	Deserializer	—	1	5 - 43	1032	1032	-40 to +105°C	TQFP-64	SERDESUR-43US SERDESUR-43SMA
8b/10b CPRI Basestation SerDes										
New SCAN12100TYA	8:1	SerDes	1	1	30.72	614.4, 1228.8		-40 to +85°C	TQFP-100	SCAN25100EVK
New SCAN25100TYA	8:1	SerDes	1	1	30.72	614.4, 1228.8, 2457.6		-40 to +85°C	TQFP-100	SCAN25100EVK
5 Gbps Bit Interleave SerDes										
SCAN50C400UT	4:1	SerDes	4	4	625	5000	20000 per direction	-40 to +85°C	TEBBGA-440	EVM50C400

Package codes: National has recently moved to 2-letter package code suffixes for new products. The new VV code refers to the same PQFP-80 package as the old VHG code.

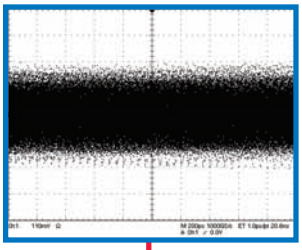
Serial Digital Interface (SDI)

SDI Signal Conditioning

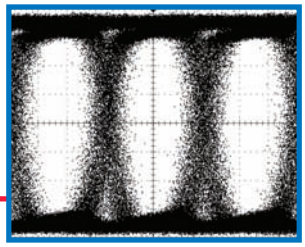
National Semiconductor offers a complete portfolio of video products for both standard definition (SD) and high definition (HD) SDI applications. National leverages its high performance analog signal conditioning expertise to provide solutions that extend cable reach, reduce jitter and transmit ultra-clean video signals that meet or exceed specifications defined by the Society of Motion Picture and Television Engineers (SMPTE).

The application example below highlights the elegant dual differential interface between the LMH0046 reclocker and LMH0202 dual cable driver. National's SDI solutions maximize performance while minimizing power consumption and space.

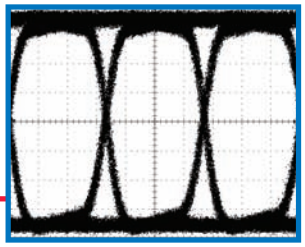
Input signal to LMH0044 after 200m cable*

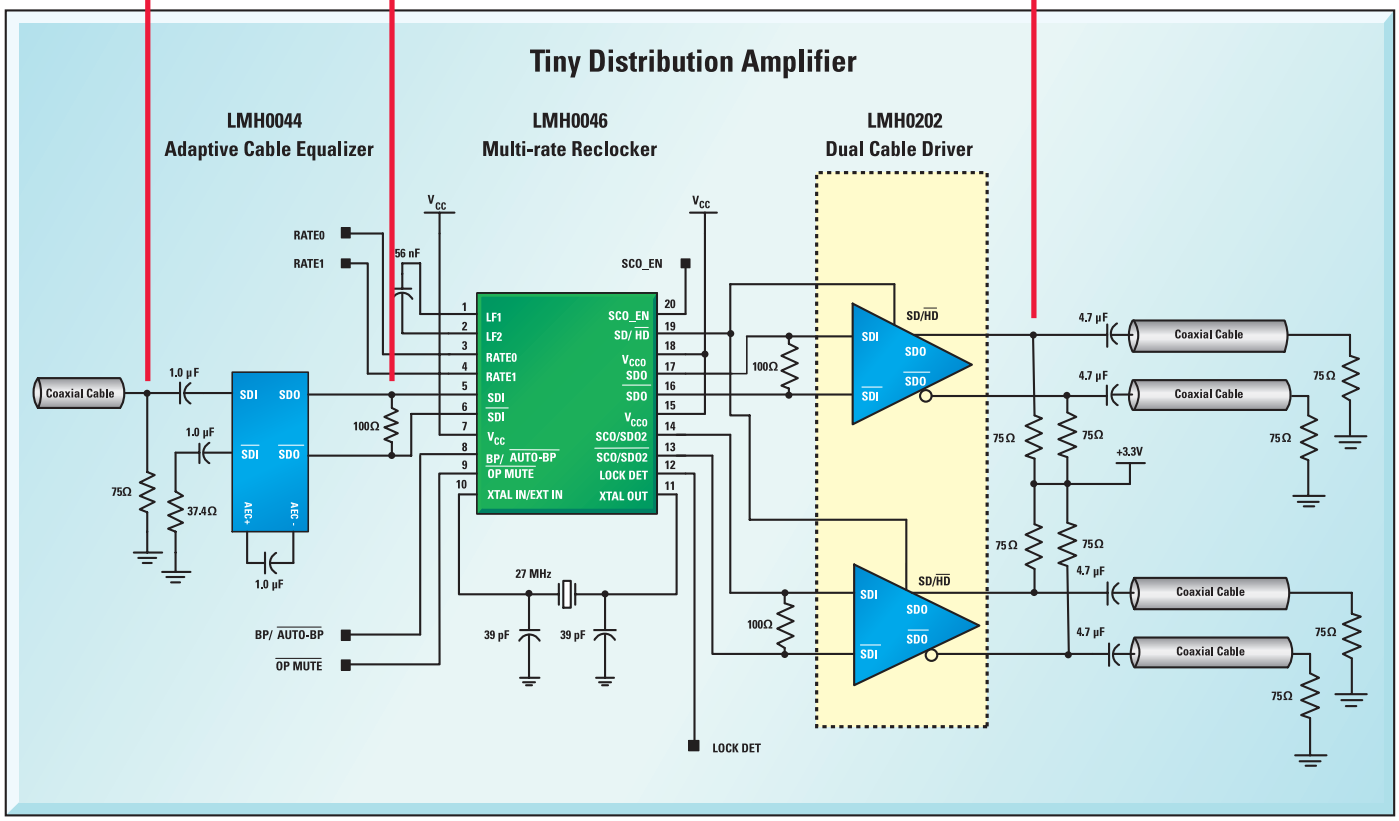


After LMH0044 105 ps p-p jitter



After LMH0046/0202 65 ps p-p jitter





* Datarate: 1.485 Gbps; cable type: Belden 1694A

Multi-Rate SDI Reclocker

Half the Power, 1/3 the Size, Double the Outputs

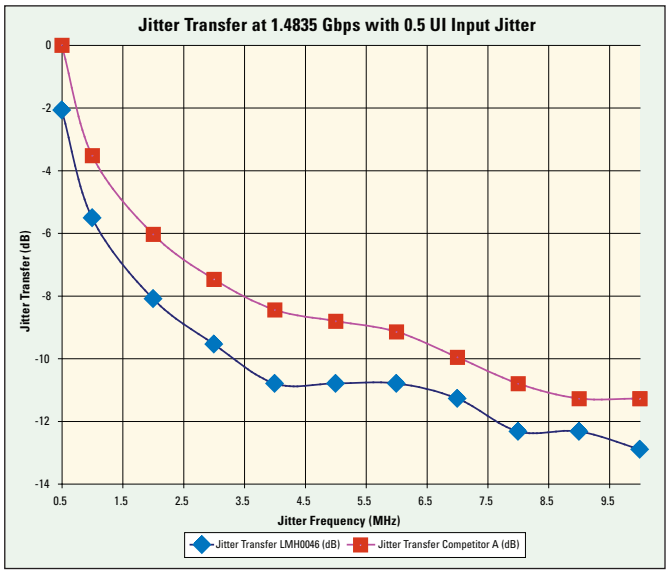
LMH0046 – HD/SD Reclocker with Dual Differential Outputs

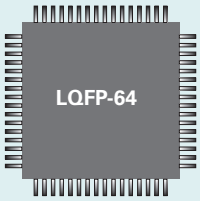
Description

National's LMH0046 is the industry's smallest, lowest power, and lowest jitter HD/SD SDI reclocker. It recovers and cleans jitter on signals with up to 60% of the "eye" closed and consumes just 330 mW typical power from a single 3.3V supply. The result: ultra-clean low-jitter data and clock with high efficiency and limited board area.

Features

- Exceeds SMPTE 259M (A & C) and SMPTE 292M serial digital video standards
- 143 Mbps, 270 Mbps, 1.483 Gbps, and 1.485 Gbps serial data rate operation
- Supports DVB-ASI at 270 Mbps
- Single 3.3V supply operation
- 330 mW typical power consumption
- Two differential, reclocked outputs
- Choice of second reclocked output or low-jitter, differential, data-rate clock output
- Single 27 MHz external crystal or reference clock input
- Industrial temperature range: -40°C to +85°C
- Differential LVPECL-compatible serial data inputs and outputs
- LVCMOS control inputs and indicator outputs
- Available in tiny TSSOP-20 packaging



	National	Competitor A	
Product ID	**LMH0046**	**Device A**	**Device B**
Number of Outputs	2	1	1
Number of Inputs	1	4 Multiplexed	4 Multiplexed
Typical Power	330	710	645
Reference Clock Frequency	27 MHz system clock or low cost 27 MHz external crystal	14.14 MHz external crystal	14.14 MHz external crystal
Package Type	TSSOP-20	QFN-64	LQFP-64
Dimensions (mm)	6.5 x 6.4	8.9 x 8.9	12 x 12
Board Area (mm^2)	41.6	79.2	144
Relative Package Size			

Typ power consumption from 3.3V supply (mW). LMH0046 is roughly one-half the size of QFN-64 and less than one-third the size of LQFP-64.

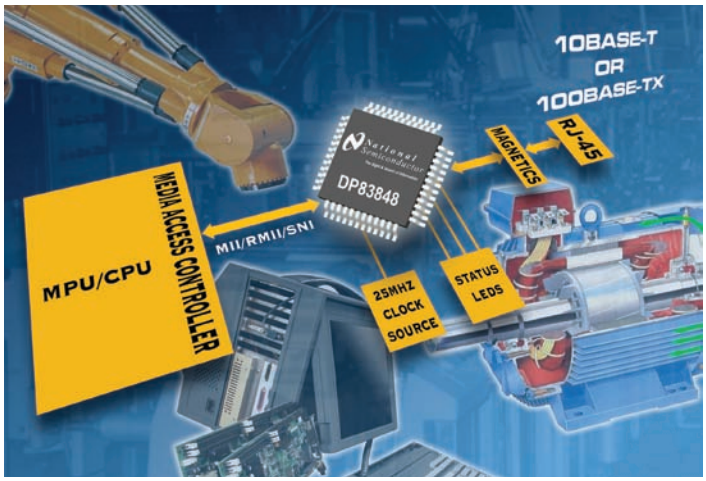
Serial Digital Interface (SDI)
Selection Table

Product ID	Function	Supply Voltage (V)	Max Speed (Mbps)	Temperature Range	Packaging	Eval Board	Comments
Cable Drivers							
CLC001AJE	SD serial cable driver with adjustable output	3.3	622	-40 to +85°C	SOIC-8	SD001EVK	Adjustable output amplitude, 3.3V
New LMH0002MA	HD/SD serial cable driver	3.3	1485	-40 to +85°C	SOIC-8	SD002EVK	Selectable slew rate
New LMH0202MT	Dual HD/SD serial cable driver	3.3	1485	0 to +70°C	TSSOP-16	SD202EVK	Dual differential input, dual differential output
CLC005AJE	SD serial cable driver	5	400	-40 to +85°C	SOIC-8	SD005EVK	ITU G.703-compliant outputs
CLC006AJE	SD serial cable driver	5	400	-40 to +85°C	SOIC-8	SD006EVK	Adjustable amplitude outputs
CLC007AJE	SD serial cable driver with complementary output pair	5	400	-40 to +85°C	SOIC-8	SD007EVK	Complementary output pair
Adaptive Equalizers							
CLC012AJE	SD adaptive cable equalizer	5	50 to 650	-40 to +85°C	SOIC-14	SD012EVK	ITU G.703-compliant recovery
CLC014AJE	SD adaptive cable equalizer	5	50 to 650	-40 to +85°C	SOIC-14	SD014EVK	SMPTE 259M serial recovery
New LMH0024MA	SD adaptive cable equalizer	3.3	143 to 1485	-40 to +85°C	SOIC-16	SD024EVK	198 mW typical power consumption, footprint compatible with LMH0034
New LMH0034MA	HD/SD adaptive cable equalizer	3.3	143 to 1485	0 to +85°C	SOIC-16	SD034EVK	Equalize 200m of cable at HD and 400m at SD data rates, manual bypass, carrier detect and output mute
New LMH0044SQ	HD/SD adaptive cable equalizer	3.3	143 to 1485	0 to +85°C	LLP-16	SD044EVK	Equalize 200m of cable at HD and 400m at SD data rates, manual bypass, carrier detect and output mute
Encoder/Decoders							
CLC011BCQ	SD serial digital video decoder	5	400	0 to +70°C	PLCC-28	SD901EVK	Data decoding and deserialization
CLC020BCQ-5.0	SD digital video serializer/encoder	5	100 to 400	0 to +70°C	PLCC-28	SD020EVK	Integrated cable driver
CLC021AVGZ-5.0	SD digital video serializer/encoder	5	400	0 to +70°C	TQFP-44	SD021-5EVK	Integrated cable driver, EDH generation/insertion
CLC021AVGZ-3.3	SD digital video serializer/encoder	3.3	400	0 to +70°C	TQFP-44	SD021-3EVK	Integrated cable driver, EDH generation/insertion
New LMH0030VS	HD/SD digital video serializer/encoder	3.3	270 to 1485	0 to +70°C	TQFP-64	SD130EVK	85 ps typical output jitter, no external VCO required, integrated cable driver, FIFO, BIST, and TPG
New LMH0031VS	HD/SD digital video deserializer/decoder	3.3	270 to 1485	0 to +70°C	TQFP-64	SD131EVK	27 MHz reference, FIFO, BIST, and TPG
Reclockers							
CLC016ACQ	SD data reclocking PLL and clock recovery	5	40 to 400	0 to +70°C	PLCC-28	SD901EVK	Automatic rate selection
CLC016AJQ / MTC	SD data reclocking PLL and clock recovery	5	40 to 400	-40 to +85°C	PLCC-28, TSSOP-28	SD901EVK	Automatic rate selection
New LMH0046MH	HD/SD reclocker with dual differential outputs	3.3	143, 270, 1483, 1485	-40 to +85°C	TSSOP-20	SD046EVK	330 mW typical power consumption, dual differential reclocked outputs
New LMH0056SQ	HD/SD reclocker with 4:1 MUX	3.3	143, 270, 1483, 1485	-40 to +85°C	LLP-48	SD056EVK	350 mW typ power consumption, 27 MHz reference, dual diff outputs
Crosspoint Switches							
CLC018AJVJQ	8 x 8 LVPECL crosspoint switch	3.3	1500	-40 to +85°C	PQFP-64	—	Non-blocking, expandable
SCAN90CP02SP/VY	2 x 2 LVDS crosspoint switch	3.3	1500	-40 to +85°C	LLP-28, LQFP-32	SCAN90CP02EVK	Programmable pre-emphasis, IEEE 1149.1/6 testability
DS90CP22M-8/MT	2 x 2 LVDS crosspoint switch	3.3	800	-40 to +85°C	SOIC-16, TSSOP-16	LVDS-CP22EVK	< 75 ps p-p Jitter, < 330 mW power
DS90CP04TLD	4 x 4 LVDS crosspoint switch	2.5	2500	-40 to +85°C	LLP-32	—	Ultra low jitter

DP83848 – PHYTER® 10/100 Ethernet PHYs for Commercial, Industrial, and Extreme Applications

Features

- Industry's lowest, deterministic latency
- Software utility support
- Selectable MII/RMII interface
- Flexible interrupt capability
- Reference clock output (to MAC)
- Controlled I/O during power up
- Very low power consumption
  < 23 mW (energy detect mode)
  < 250 mW (normal operation)
- Built-in Self-Test (Packet BIST)
- Fully IEEE 802.3u compliant
- Available in space-saving 7 x 7 mm LQFP-48 packaging, and 6 x 6 mm LLP-40 packaging

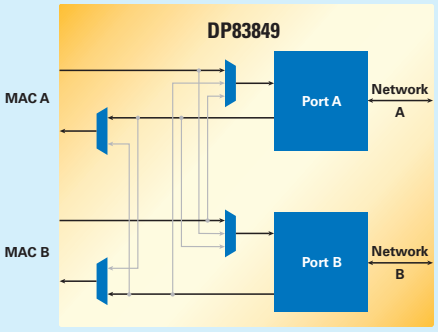


	PHYTER (Single)			PHYTER Mini (Single, Tiny Package) New		
Parameter	**Commercial**	**Industrial**	**Extreme**	**Commercial**	**Industrial**	**Extreme**
Product ID	DP83848C	DP83848I	DP83848YB	DP83848M/J	DP83848T/K	DP83848H
Temp Range (°C)	0 to +70	-40 to +85	-40 to +125	0 to +70	-40 to +85	-40 to +125
Number of Ports	Single	Single	Single	Single	Single	Single
Interface	MII/RMII/SNI	MII/RMII/SNI	MII/RMII/SNI	MII	MII	MII
Power	265 mW	265 mW	265 mW	265 mW	265 mW	265 mW
IEEE 802.3 Compliant	•	•	•	•	•	•
UNH Interoperability Testing	•	•	•	•	•	•
Auto-MDIX	•	•	•	•	•	•
Real-Time Ethernet						
Deterministic Delay	•	•	•	•	•	•
Low Latency	•	•	•	•	•	•
LEDs	3	3	3	1 (DP83848M) 2 (DP83848J)	1 (DP83848T) 2 (DP83848K)	2
Interrupt Pin	•	•	•			
Fiber Support						
Flexible Port Switching						
Cable Health Diagnostics						
System Diagnostics	•	•	•	•	•	•
IEEE 1149.1 (JTAG)		•	•			
Software Utility Support	•	•	•	•	•	•
Error-Free Operation (m typ)	137	150	150	137	137	137
Supply Voltage (V)	3.3	3.3	3.3	3.3	3.3	3.3
Package	LQFP-48	LQFP-48	LQFP-48	LLP-40	LLP-40	LLP-40
Package Size (mm)	9 x 9 x 1.4	9 x 9 x 1.4	9 x9 x 1.4	6 x 6 x 0.8	6 x 6 x 0.8	6 x 6 x 0.8
ESD HBM/CDE (kV)	4.0 / 2.0	4.0 / 2.0	4.0 / 2.0	4.0 / 2.0	4.0 / 2.0	4.0 / 2.0

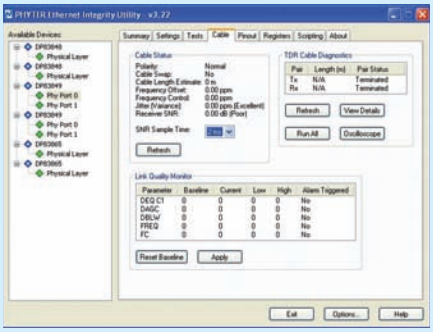
DP83849 – Dual PHYTER 10/100 Ethernet PHY for Commercial, Industrial, and Fiber Applications

Features

- Flexible port switching and chaining
  - MII port assignment
  - MDI chaining
- Industry's lowest, deterministic latency
- Enhanced cable diagnostics
- Two fully independent 10/100 ports
  - Selectable 100Base-Tx/100Base-Fx
  - MII/RMII/SNI
- Controlled I/O during power up
- Built-in Self-Test (Packet BIST)
- Industrial temperature range
- Fully IEEE 802.3u compliant
- Available in 12 x 12 mm TQFP-80 packaging
- Low power consumption: < 300 mW per port



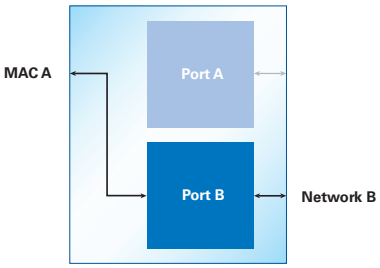
Unique Flexible Switching Capability



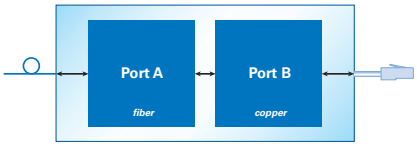
Enhanced Cable Diagnostics

Parameter	PHYTER Dual (New) Commercial	Industrial	Fiber Support	Fiber Support
Product ID	DP83849C	DP83849I	DP83849ID	DP83849IF
Temp Range (°C)	0 to +70	-40 to +85	-40 to +85	-40 to +85
Number of Ports	Dual	Dual	Dual	Dual
Interface	MII/RMII	MII/RMII	MII/RMII	MII/RMII
Power	300 mW/port	300 mW/port	300 mW/port	300 mW/port
IEEE 802.3 Compliant	•	•	•	•
UNH Interoperability Testing	•	•	•	•
Auto-MDIX	•	•	•	•
Real-Time Ethernet				
Deterministic Delay	•	•	•	•
Low Latency	•	•	•	•
LEDs	3	3	3	3
Interrupt Pin	•	•	•	•
Fiber Support			•	•
Flexible Port Switching		•		•
Cable Health Diagnostics	•	•	•	•
System Diagnostics	•	•	•	•
IEEE 1149.1 (JTAG)		•	•	•
Software Utility Support	•	•	•	•
Error-Free Operation (m typ)	137	137	137	137
Supply Voltage (V)	3.3	3.3	3.3	3.3
Package	TQFP-80	TQFP-80	TQFP-80	TQFP-80
Package Size (mm)	12 x 12 x 1.0	12 x 12 x 1.0	12 x 12 x 1.0	12 x 12 x 1.0
ESD HBM/CDE (kV)	4.0 / 2.0	4.0 / 2.0	4.0 / 2.0	4.0 / 2.0

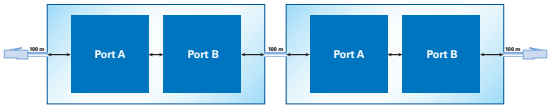
Other Useful DP83849 Configurations



Failover Operation



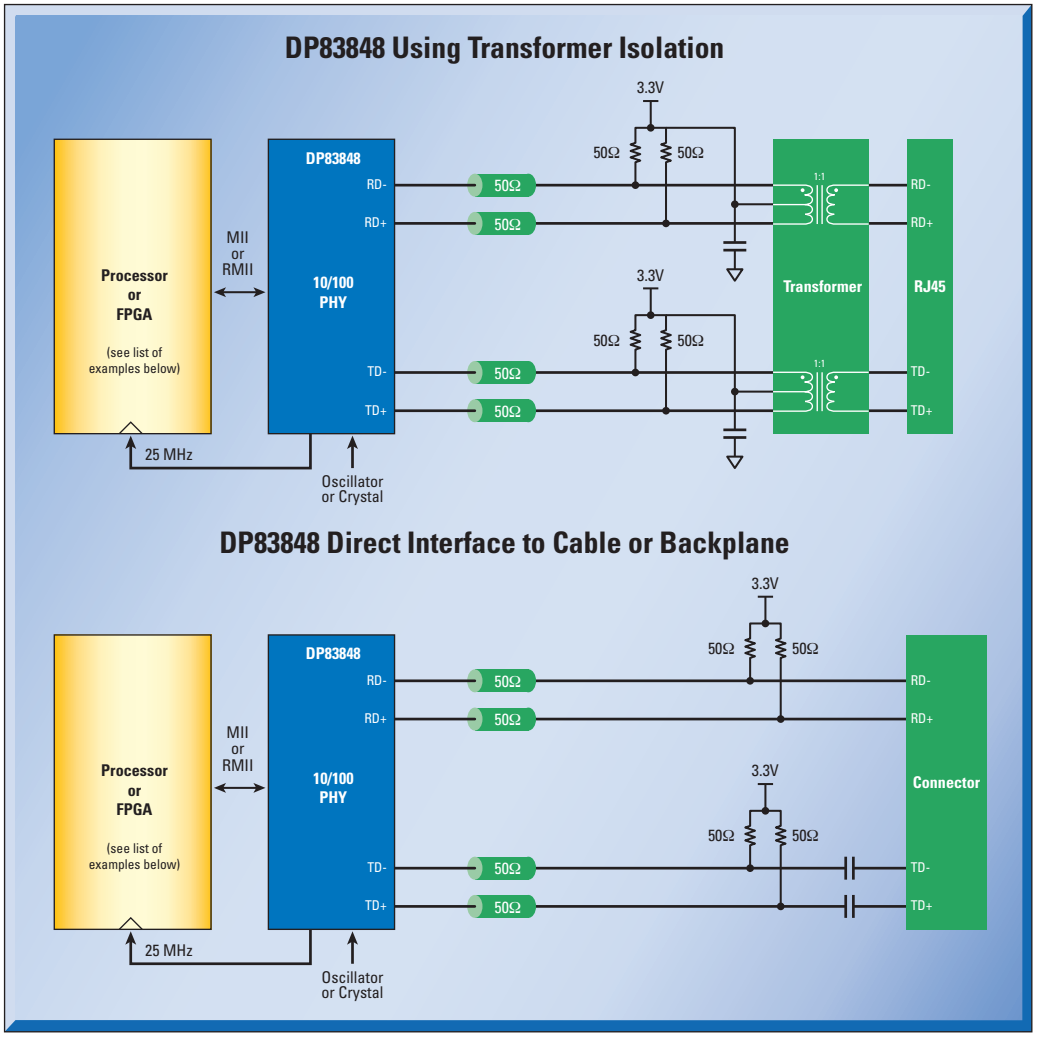
Fiber-Copper Converter (MAC-less)



300 m Repeater-Extender (MAC-less)

High-Speed Industrial Connectivity Made Easy

Advanced 10/100 PHYs



Selected Processors and FPGAs Available with Integrated 10/100 MAC

Freescale ColdFire Processors
MCF5207
MCF5208†
MCF523x
MCF527x
MCF528x (e.g. MCF5282†)
MC5328/9†
MCF537x
MCF547x
MCF548x
MCF7113/6/9

† DP83848 reference design available

Freescale PowerQUICC Processors
MPC68xx
MPC8xx (selected parts)
MPC82xx
MPC83xx
MPC85xx
MPC52xx

IBM PowerPC Processors
PowerPC 440GP†

† DP83848 reference design available

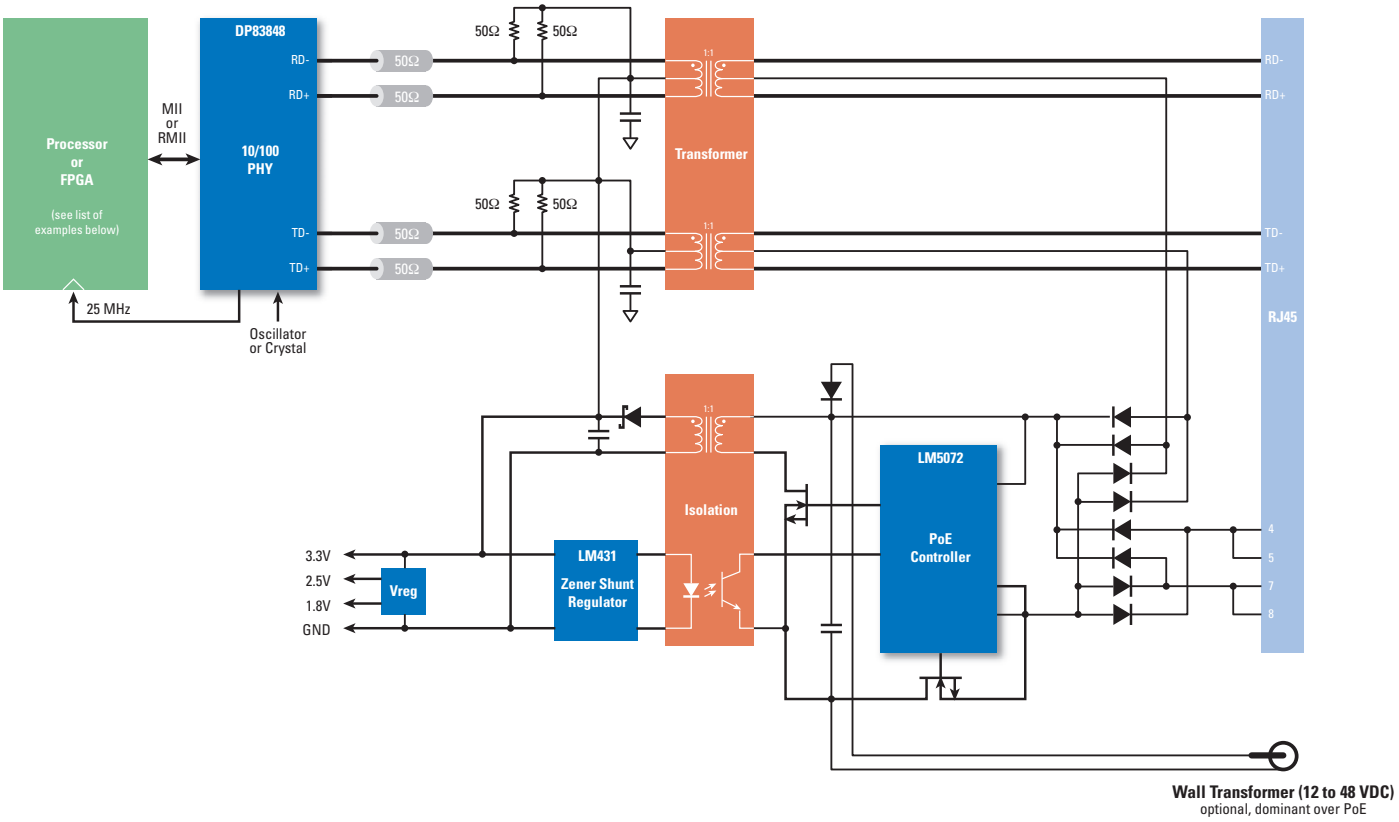
Altera FPGA Families
APEX 20K
Stratix and Stratix II
Stratix GX and Stratix II GX
Cyclone and Cyclone II

Xilinx FPGA Families
Virtex-4 SX/LX/FX
Virtex-II and Virtex-II Pro
Virtex
Spartan-3/3E/IIE/II

NXP Controllers
LPC23xx

Complete 10/100 Power-over-Ethernet Solution

DP83848 10/100 Ethernet PHY + LM5072 PoE Controller



LM5072

Integrated 100V Power-over-Ethernet (PoE) PD Interface and PWM Controller with Aux Support

PD Interface

- Fully compliant IEEE 802.3af PD interface
- Versatile auxiliary power options
- 9V minimum auxiliary power operating range
- 100V maximum input voltage rating
- Programmable DC current limit up to 800 mA
- 100V, 0.7 hot swap MOSFET
- Integrated PD signature resistor
- Integrated PoE input UVLO
- Programmable inrush current limit
- PD classification capability
- Power good indicator
- Thermal shutdown protection

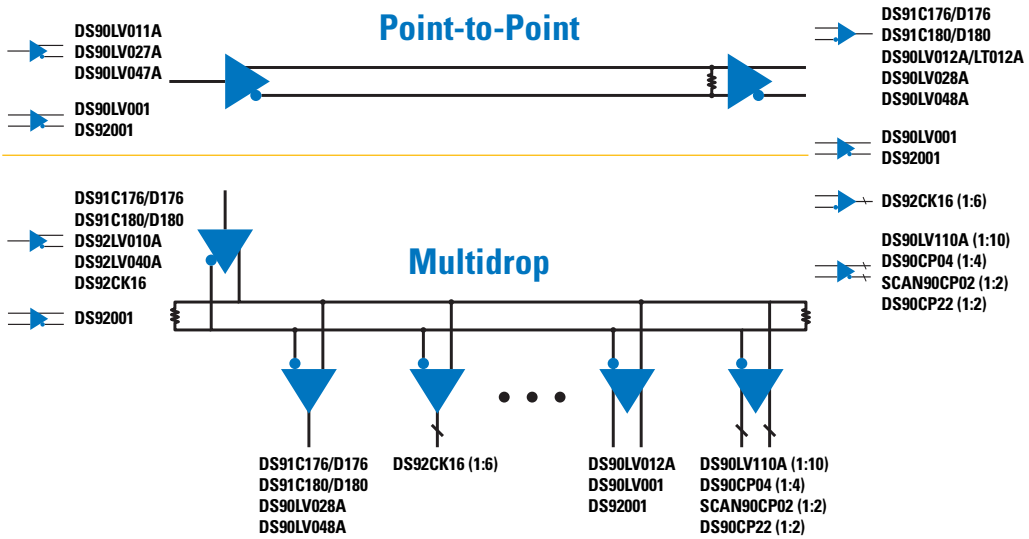
PWM Controller

- Current mode PWM controller
- 100V start-up regulator
- Error amplifier with 2% voltage reference
- Supports isolated and non-Isolated applications
- Programmable oscillator frequency
- Programmable soft-start
- 800 mA peak gate driver
- 80% maximum duty cycle with built-in slope compensation (-80 device)
- 50% maximum duty cycle, no slope compensation (-50 device)

Timing Products
LVDS Clock Distribution

National offers a comprehensive range of products for clock distribution from high speed, low jitter point-to-point LVDS buffers and translators to slow edge rate M-LVDS and Bus LVDS drivers for multidrop applications. Splitters and crosspoints create multiple copies of your clock or can be used for clock redundancy.

The diagram helps you to quickly find the right clock drivers and receivers for your application.

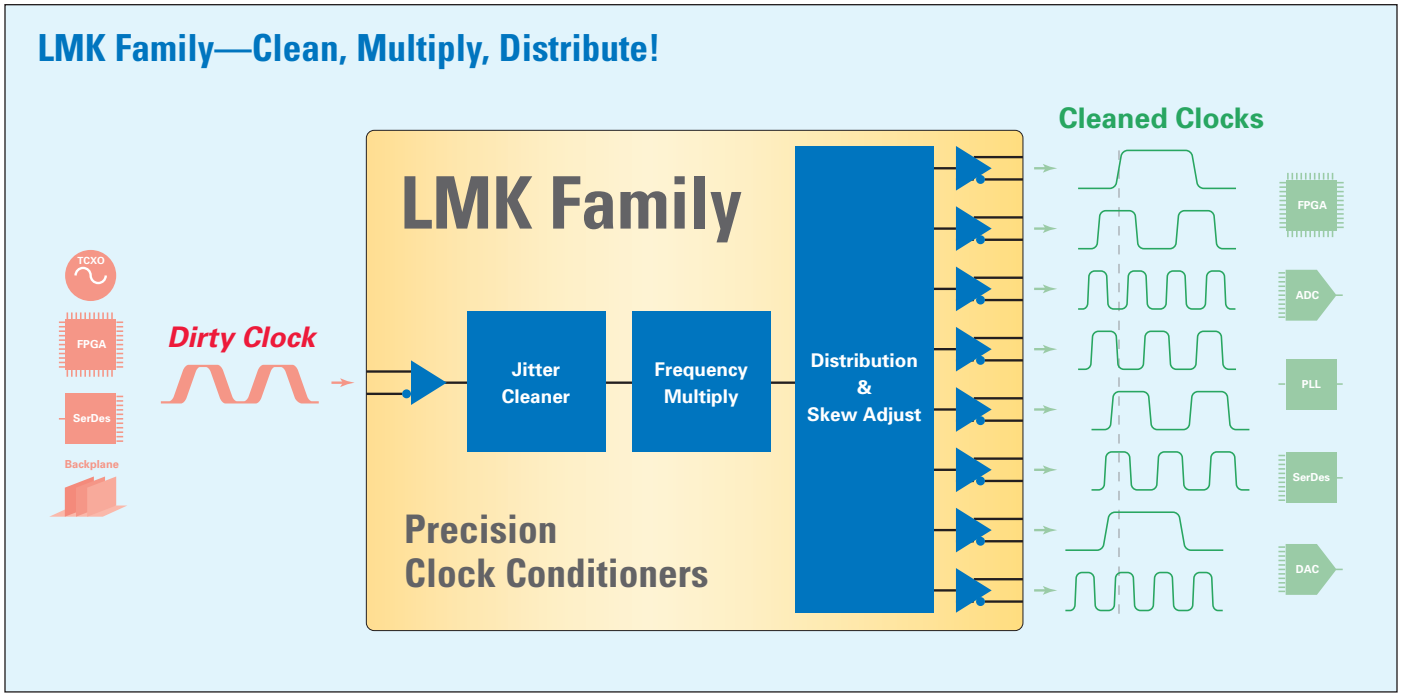


Part Number	Drivers	Receivers	Input Compatibility	Output	Max Clock (MHz)	Packaging	Comments
Point-to-Point Drivers							
DS90LV001TM/TLDA	1	1	LVDS/LVPECL/CML	LVDS	400	SOIC/LLP-8	Low jitter, high quality LVDS output
DS92001TM/TLD	1	1	LVDS/LVPECL/CML	Bus LVDS	200	SOIC/LLP-8	Controlled edge rates, LOS flag
DS90LV011ATMF/ATLD	1	0	LVTTL/LVCMOS	LVDS	200	SOT23-5, LLP-8	Flow-through pinout, tiny packages
DS90LV027ATM	2	0	LVTTL/LVCMOS	LVDS	200	SOIC-8	Flow-through pinout
DS90LV047ATM/ATMTC	4	0	LVTTL/LVCMOS	LVDS	200	SOIC/TSSOP-16	Flow-through pinout
Multidrop Drivers							
New DS91C176TM/D176TM	1	1	M-LVDS/LVDS	M-LVDS	100	SOIC-8	Half duplex, controlled edge rates
New DS91C180TM/D180TM	1	1	M-LVDS/LVDS	M-LVDS	100	SOIC-14	Full duplex, controlled edge rates
DS92LV010ATM	1	1	LVDS/LVPECL/CML	Bus LVDS	80	SOIC-8	3.3V or 5V operation
DS92001TM/TLD	1	1	LVDS/LVPECL/CML	Bus LVDS	200	SOIC/LLP-8	Controlled edge rates, LOS flag
DS92LV040ATLQA	4	4	LVDS/LVPECL/CML	Bus LVDS	100	LLP-44	Controlled edge rates, low skew
1:1 Receivers							
New DS91C176TM/D176TM	1	1	M-LVDS/LVDS	M-LVDS	100	SOIC-8	Half duplex, type 2/1 wide common mode input
New DS91C180TM/D180TM	1	1	M-LVDS/LVDS	M-LVDS	100	SOIC-14	Full duplex, type 2/1 wide common mode input
DS90LV012ATMF/ATLD	0	1	LVDS/LVPECL/CML	LVTTL	200	SOT23-5, LLP-8	Flow-through pinout, tiny packages
DS90LT012ATMF/ATLD	0	1	LVDS/LVPECL/CML	LVTTL	200	SOT23-5, LLP-8	Flow-through pinout, integrated termination
DS90LV028ATM	0	2	LVDS/LVPECL/CML	LVTTL	200	SOIC-8	Flow-through pinout
DS90LV048ATM/ATMTC	0	4	LVDS/LVPECL/CML	LVTTL	200	SOIC/TSSOP-16	Flow-through pinout
1:n Receivers							
SCAN90CP02SP/VY	2	2	LVDS/LVPECL/CML	LVDS	750	LLP-28/ LQFP-32	Programmable pre-emphasis, JTAG, 1149.6
DS90CP04TLD	4	4	LVDS/LVPECL/CML	LVDS	1250	LLP-32	Very low jitter, small footprint
DS92CK16TMTC	1	6	LVDS or LVTTL	LVTTL and Bus LVDS	125	TSSOP-24	Configurations: A) LVTTL input to 6 LVTTL + 1 BLVDS outputs B) LVDS input to 6 LVTTL outputs
DS90LV110ATMT	1	10	LVDS/LVPECL/CML	LVDS	200	TSSOP-28	Low output jitter

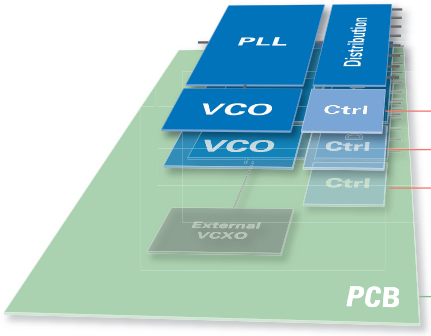
Note: the products above are characterized over the full -40 to +85°C industrial temperature range.

LMK Clock Conditioner Family

Jitter Cleaning + Multiplication + Distribution



- Clean: Jitter reduced to as low as 0.2 ps RMS typ
- Multiply/divide: Outputs up to 785 MHz from ≤ 200 MHz input
- Distribute: 3 LVDS plus 5 LVPECL individually frequency- & skew- programmable outputs
- Integrated VCO saves cost and board space
- Three performance grades, one pinout/PCB
- Easy to use



Grade	Jitter (RMS typ)
Standard	0.8 ps
Premium	0.4 ps
External VCXO	0.2 ps

One PCB Layout

Product ID	LVDS Outputs	LVPECL Outputs	VCO	PLL	VCO Frequency	Jitter (RMS typ)
New LMK02000	3	5	External VCXO	Integrated	—	0.2 ps†
New LMK03000C	3	5	Integrated	Integrated	1185 to 1296 MHz	0.4 ps
New LMK03001C	3	5	Integrated	Integrated	1500 to 1600 MHz	0.4 ps
New LMK03000	3	5	Integrated	Integrated	1185 to 1296 MHz	0.8 ps
New LMK03001	3	5	Integrated	Integrated	1500 to 1600 MHz	0.8 ps

Pin Compatible

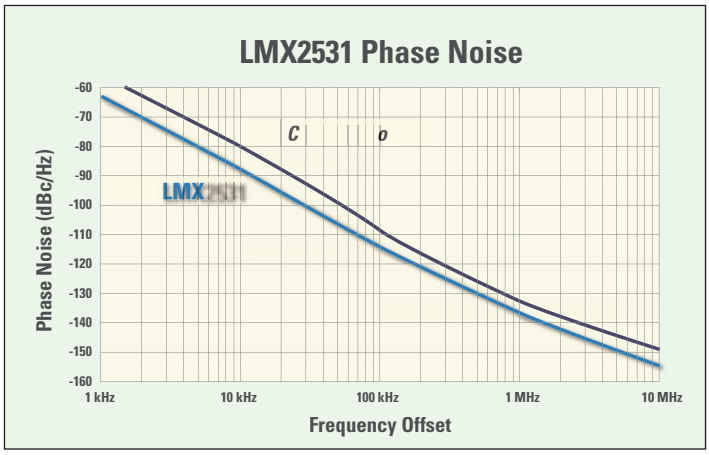
† 0.2 ps including external VCXO

LMX2531

PLLatinum® Frequency Synthesizer System with Integrated VCO

Features

- 765 to 2790 MHz range in multiple frequency options
- Up to 10 dB improvement over next best monolithic competitor
- Significant cost savings over discrete and module solutions
- Fractional-N PLL programmable up to 4th order
- Low 34 mA typ power consumption
- High +4 dB typ output power simplifies external matching circuitry and buffering
- Fast lock, cycle slip reduction with timeout counter
- Partially integrated adjustable loop filter
- Very low phase noise and spurs
- Low phase noise VCO with integrated tank inductor and programmable output power level
- 2.8 to 3.2V operation
- Very low power down current
- 1.8V MICROWIRETM support
- Available in tiny 6 x 6 mm LLP-36 packaging



Parameter	LMX2531	Competitor A
Phase Noise (at F_{OUT} = 2 GHz, offset = 100 kHz)	-116 dBc/Hz	-107 dBc/Hz
PLL	Fractional-N ΔΣ	Integer
Loop Filter	Partially Integrated	External
Power Consumption	35/40 mA typ/max	50 mA typ
Output Power	+4 dBm typ	-6 dBm typ
Supply Voltage	2.8 to 3.2V	3.0 to 3.6V

Product ID	Low Band (MHz)	High Band (MHz)
New LMX2531LQ1500E	749.5 - 755	1499 to 1510
LMX2531LQ1570E	765 to 818	1530 to 1636
LMX2531LQ1650E	795 to 850	1590 to 1700
LMX2531LQ1700E	831 to 885	1662 to 1770
LMX2531LQ1742	880 to 933	1760 to 1866
LMX2531LQ1778E	863 to 920	1726 to 1840
LMX2531LQ1910E	917 to 1014	1834 to 2028
LMX2531LQ2080E	952 to 1137	1904 to 2274
LMX2531LQ2265E	1089 to 1200	2178 to 2400
LMX2531LQ2570E	1168 to 1395	2336 to 2790

Other frequency bands in development and by request

Timing Products	
WEBENCH	EasyPLL WEBENCH Design Tool
Handbook	PLL Performance, Simulation and Design Handbook 4th Edition
AN-884	Integrated LNA and Mixer Basics
AN-1001	An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge Pump PLLs
AN-1006	Phase-Locked Loop Based Clock Generators
Web Seminar	Advantages and Pitfalls of Using Fractional N PLLS
Web Seminar	PLL Loop Filter Optimization
Web Seminar	Non-PLL Radio Frequency (RF) Basics
Web Seminar	PLL Building Blocks
Web Seminar	PLL Performance
Web Seminar	Fractional PLLs
Web Seminar	National's PLL Tools
Web Seminar	Advanced PLL Concepts
Article	The Impact of Various PLL Parameters on System Performance
Application Brief	Delta Sigma PLLs Raise The Standard For Performance
Evaluation Boards	Visit: wireless.national.com
Software	PLL Codeloader Evaluation Software
Reading Lists	List of literature for further reading about PLLs
Discussion Forum	Visit: www.national.com/national/wirelessMB.nsf

PLL Products
Selection Table

High-Performance PLLatinum™ Family of PLL Products

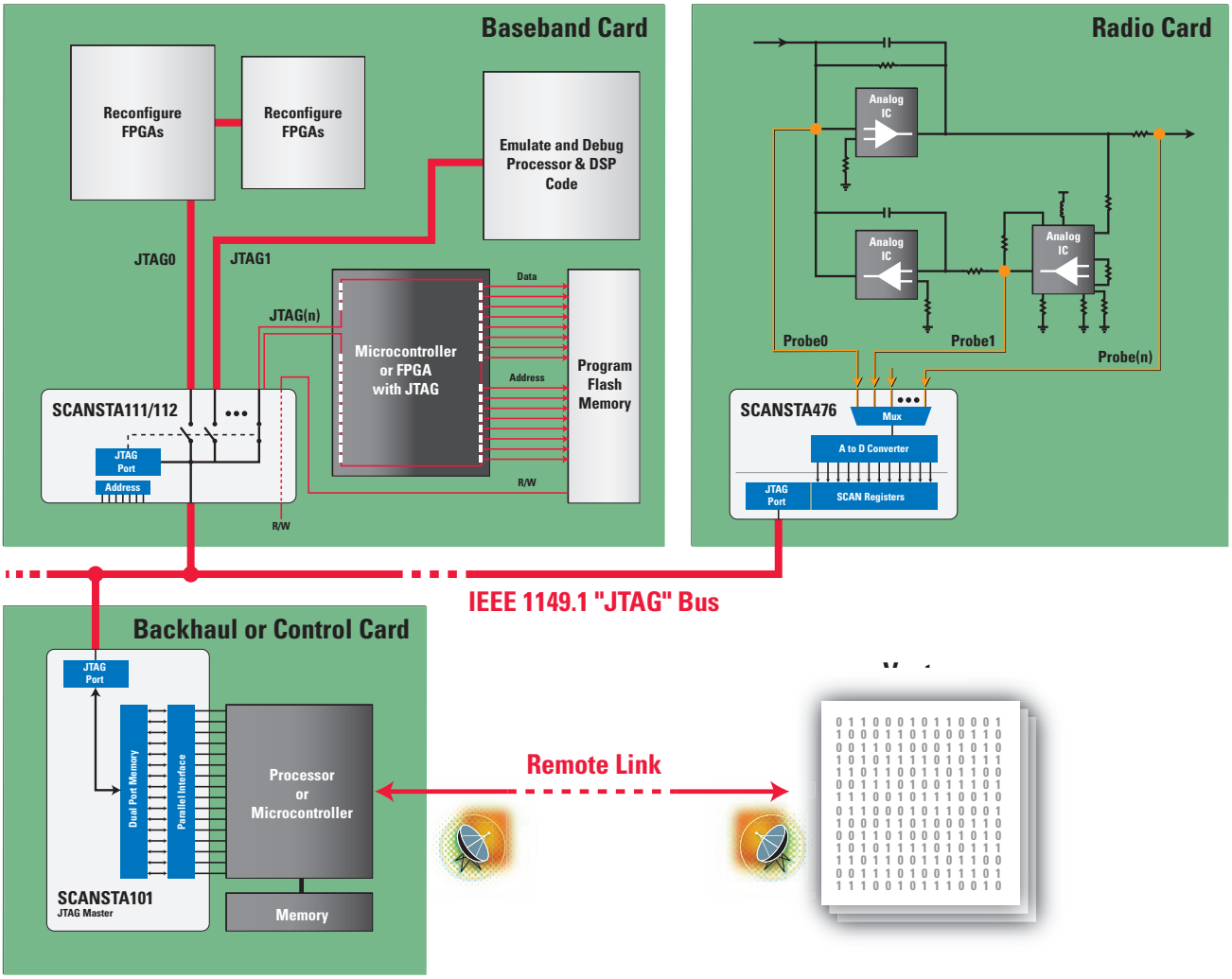
Part Number	Main Operating Frequency Range (GHz)	Aux. Operating Frequency Range (MHz)	Main Normalized Phase Noise (dBc/Hz)	Supply Current (mA)	Supply Voltage (V)	Package Size (mm)
Single Integer PLLs						
LMX2310U	0.5 to 2.5	—	-212	2.3	2.7 to 5.5	3.5 x 3.5 x 0.8
LMX2347	0.2 to 2.5	—	-217	3.6	2.7 to 5.5	3.5 x 3.5 x 0.6
LMX2311U	0.5 to 2.0	—	-212	2.0	2.7 to 5.5	3.5 x 3.5 x 0.8
LMX2346	0.2 to 2.0	—	-217	3.0	2.7 to 5.5	3.5 x 3.5 x 1.0
LMX2312U	0.2 to 1.2	—	-212	1.4	2.7 to 5.5	3.5 x 3.5 x 0.8
LMX2313U	45 to 600 MHz	—	-212	1.0	2.7 to 5.5	3.5 x 3.5 x 0.8
Dual Integer PLLs						
LMX2434	1.0 to 5.0	500 to 2500	-219	7.0	2.35 to 2.75	3.5 x 3.5 x 0.6
LMX2433	0.5 to 3.6	250 to 1700	-219	5.2	2.25 to 2.75	3.5 x 3.5 x 0.6
LMX2430	0.25 to 3.0	100 to 800	-219	4.2	2.25 to 2.75	3.5 x 3.5 x 0.6
Fractional-N PLLs						
New LMX2487	3.0 to 6.0	250 to 3000	-209	8.2	2.5 to 3.6	4.0 x 4.0 x 0.75
New LMX2486	1.0 to 4.5	250 to 3000	-210	8.3	2.5 to 3.6	4.0 x 4.0 x 0.75
New LMX2485	0.5 to 3.0	75 to 800	-209	5	2.5 to 3.6	4.0 x 4.0 x 0.75
New LMX2485E	0.05 to 3.0	75 to 800	-209	5	2.5 to 3.6	4.0 x 4.0 x 0.75
LMX2470	0.5 to 2.6	75 to 800	-210	4.1	2.25 to 2.75	4.5 x 3.5 x 0.6
LMX2354	0.5 to 2.5	10 to 550	-204	6	2.7 to 5.5	4.5 x 3.5 x 1.0

JTAG: More Than Board Test

Remote Diagnostic and Reconfiguration Solutions

Quickly Target and Reprogram FPGAs and Flash; Emulate and Debug Processor and DSP Code

Monitor Critical Analog Voltages



Remotely Manage, Diagnose, and Reconfigure System

JTAG System Management Products

Part Number	Description	Supply Voltage	Features	Packaging
SCANSTA111MT/SM	3-Port multidrop IEEE 1149.1 "JTAG" bus multiplexer	3.3	7 address inputs, 3 local scan ports, transparent mode	TSSOP-48, BGA-49
New SCANSTA112VS/SM	7-Port multidrop IEEE 1149.1 "JTAG" bus multiplexer	3.3	8 address inputs, 7 local scan ports, transparent mode, stitcher mode	TQFP-100, BGA-100
SCANSTA101SM	IEEE 1149.1 "JTAG" system test master	3.3	Parallel 16-bit interface to IEEE 1149.1 master device	BGA-49
New SCANSTA476TSD	8-Input IEEE 1149.1 "JTAG" analog voltage monitor	2.7 to 5.5	8 selectable analog 0-V_{DD} input channels, 2 mV typ accuracy	LLP-16

Solution Finder
By System and Application

System	Requirement	Solution	Page
Imaging	Cable: ≤ 20m	• 10-, 16-, 18-, and 24-bit embedded clock SerDes	11-13
	Cable: ≤ 400m	• DS15BA101/DS15EA101 (≤ 1.5 Gbps) • Ethernet DP83848/DP83865	8-10 17-20
	Camera link	• Channel Link SerDes	12
Wireless Infrastructure	Data bus	• 10-, 16-, 18-, and 24-bit embedded clock SerDes	11-13
	Control bus	• Ethernet and M-LVDS	17-20, 5-6
	Test bus	• SCANSTA101/111/112/476	25
	Clock	• Clock distribution, synthesis, and conditioning	21-24
Telecom/Datacom	Data bus	• 10-, 16-, 18-, and 24-bit embedded clock SerDes • Ethernet	11-13 17-20
	Control bus	• LVDS, M-LVDS, and CML drivers, receivers, and buffers	5-10
	Test bus	• SCANSTA101/111/112/476	25
	Signal conditioning	• Signal conditioners (pre-emphasis, equalization, etc.)	7-10
	Switching/redundancy	• DS42MB200, DS15MB200 • LVDS crosspoints, muxes, and buffers	8-10
	Clock	• Clock distribution, synthesis, and conditioning	21-24
	GalNet-2 switch stacking bus	• DS90CR217/218A Channel Link SerDes	12
Printers/Copiers	SerDes	• 21-, 28-, and 48-bit Channel Link SerDes, 24-bit SerDes	12-13
	Buffer	• LVDS and CML drivers, receivers, and buffers	5-10
Broadcast Video	Data bus	• SDV serializers, cable drivers, equalizers, reclockers, etc. • LVDS crosspoints, muxes, and buffers	14-16 9-10
	Clock	• Clock distribution, synthesis, and conditioning	21-24
Displays (Industrial/Commercial)	0 to 20m	• 10-, 16-, 18-, and 24-bit embedded clock SerDes (n:1) • Channel Link SerDes (n:m compression)	11-13
	20 to 300m	• DS15BA101/DS15EA101	8-10
Industrial (e.g. test, data acquisition, metering, etc)	Data bus	• 10-, 16-, 18-, and 24-bit embedded clock SerDes • 21-, 28-, and 48-bit Channel Link SerDes	11-13
	Control bus	• Ethernet • LVDS, M-LVDS	17-20, 5-6
	Clock	• Clock distribution, synthesis, and conditioning	21-24
Automotive	Displays	• 24-bit embedded clock SerDes	12

Application	Requirement	Solution	Page
FPGA/ASIC Signal Boosting	Driver signal boost	• LVDS and CML drivers, receivers, and buffers	5-10
	Tight receiver threshold	• LVDS and CML drivers, receivers, and buffers	5-10
	Receiver equalization	• Signal conditioners (pre-emphasis, equalization, etc.)	7-10
	Switching/redundancy	• DS42MB2, DS15MB200 • LVDS crosspoints, muxes, and buffers	8-10
Ribbon Cable Replacement	≤ 20m	• 10-, 16-, 18-, and 24-bit embedded clock SerDes (n:1) • 21-, 28-, and 48-bit Channel Link SerDes (n:m compression)	11-13
Clocks	Point-to-point and multidrop distribution Clock Conditioning PLL Clock Synthesis	• LVDS, M-LVDS, and CML drivers, receivers, and buffers • LVDS crosspoints, muxes, and buffers • LMK family of clock conditioners • PLLatinum PLLs and PLL/VCOs	21 10 22 23-24
Level Translation	LVDS-LVPECL-CML	• LVDS and LVPECL buffers	10
Switching/Redundancy	1:n, n:1, n:m	• DS42MB200, DS15MB200 • LVDS crosspoints, muxes, and buffers	8-10
Cable: ≤ 20m	Buffer	• Signal conditioners	7-10
	SerDes	• 10-, 16-, 18-, and 24-bit embedded clock SerDes (n:1) • 21-, 28-, and 48-bit Channel Link SerDes (n:m compression)	11-13
Cable: ≤ 400m	≤ 1.5 Gbps	• DS15BA101/DS15EA101	8-10
Backplane	SerDes	• 10-, 16-, 18-, and 24-bit embedded clock SerDes (n:1) • 21-, 28-, and 48-bit Channel Link SerDes (n:m compression)	11-13
	Signal conditioning	• Signal conditioners (pre-emphasis, equalization, etc.)	7-10
	Switching/redundancy	• DS42MB200, DS15MB200 • LVDS crosspoints, muxes, and buffers	8-10
JTAG System Test	1:n JTAG bus multiplexing	• SCANSTA111/112 3/7-port multidrop IEEE 1149.1 mux	25
	Health monitoring	• SCANSTA476 IEEE 1149.1 analog voltage monitor	25
	µP/µC to JTAG bus converter	• SCANSTA101 16-bit to IEEE 1149.1 bus converter	25
FPGA and Flash Programming	JTAG chain routing	• SCANSTA111/112 3/7-port multidrop IEEE 1149.1 mux	25

Design Resources
LVDS.national.com

Type	Description
LVDS PHYs	
Design Guide	LVDS Owner's Manual
Web Seminar	Basics of LVDS
Web Seminar	Introduction to LVDS
Web Seminar	The Many Flavors of LVDS
Web Seminar	LVDS Bus Configurations (point-to-point, multidrop, and multipoint)
Web Seminar	Bus LVDS Signaling
Web Seminar	Understanding Transmission Lines and How to Design Them
Web Seminar	Links to Industry Standards
AN-905	Transmission Line RAPIDESIGNER Operation and Applications Guide
AN-971	Introduction to LVDS
AN-977	Signal Quality - Eye Patterns
AN-1040	Bit Error Rate Testing - DS90C031
AN-1060	LVDS - Megabits @ milliwatts (EDN Reprint)
AN-1088	Signal Quality - DS90LV017/27 and DS92LV010A
AN-1110	Power Dissipation of LVDS Drivers and Receivers
AN-1115	Bus LVDS and DS92LV010A Transceiver
AN-1123	Sorting out Backplane Driver Alphabet Soup
AN-1173	High Speed Bus LVDS Clock Distribution Using the DS92CK16 Clock Distribution Device
AN-1194	Failsafe Biasing of LVDS Interfaces
AN-1503	Designing an AdvancedTCA Compliant M-LVDS Clock Distribution Network
White Paper	A Baker's Dozen of High-Speed Differential Backplane Design Tips
White Paper	Bus LVDS Expands Applications for Low Voltage Differential Signaling (LVDS)
White Paper	Signal Integrity and Validation of Bus LVDS (BLVDS) Technology in Heavily Loaded Backplanes
LVDS47/48EVK	DS90LVxxx Evaluation Board
Software	IBIS and BSDL Models
High-Speed Industrial 10/100 Connectivity	
Schematic Review	www.national.com/appinfo/networks/webench/dp83848.html
AN-1401	DP83848 Energy Detect Mode
AN-1402	DP83848 Initialization During Power Down Mode
AN-1405	DP83848 Reduced Media Independent Interface™ (RMII™) Mode
AN-1425	DP8384x Differences Between National 10/100 Mb/s Ethernet Physical Layer Devices
AN-1470	DP83847 to DP83848C/I/YB PHYTER Mini System Rollover Document
AN-1499	DP83846 to DP83848C/I/YB PHYTER System Rollover Document
Software	PHYTER® Ethernet Integrity Utility Tool
Software	IBIS and BSDL Models
Reference Design	DP83848 Demo Boards

Type	Description
JTAG	
BSDL Models	http://www.national.com/appinfo/scan
AN-1327	Simplified Programming of Altera FPGA's using a SCANSTA111/112 Scan Chain Mux
AN-1340	Simplified Programming of Xilinx FPGA's using a SCANSTA111/112 Scan Chain Mux
AN-1312	STA111/STA112 Timing
AN-1313	SCAN90CP02 Design for Test (DfT) Features
AN-1259	SCANSTA112 Designers Reference
AN-121	Partition IEEE 1149.1 SCAN Chains for Manageability
AN-891	Non-Contact Test Access for Surface Mount Technology
AN-890	P1149.1A Extensions to IEEE-Std-1149.1-1990
Web Seminar	Boundary SCAN Enables System Level Programming, Configuration, and Mixed-Signal Test
White Paper	Using At-Speed BIST To Test LVDS Serializer/Deserializer Function
White Paper	JTAG, Design for Test (DfT), and the Testability Question
White Paper	Satellite Hierarchical System Test Using IEEE 1149.1-Based COTS Test Tools: A Case History with Results and Lessons
White Paper	Preliminary Results of Passive Component Measurement Methods Using an IEEE 1149.4 Compliant Device from the Board Test Workshop 2002
SerDes	
Design Guide	Channel Link Design Guide
Design Guide	DS92LV16 16-bit SerDes Design Guide
Design Guide	DS92LV18, SCAN921821 18-bit SerDes Design Guide
AN-1041	Introduction to Channel Link
AN-1108	PCB and Interconnect Design Guidelines
AN-1109	Multi-drop Application of Channel Links
White Paper	SerDes Architectures and Applications
AN-905	Transmission Line RAPIDESIGNER Operation and Applications Guide
AN-1217	How to Validate BLVDS SerDes Signal Integrity Using an Eye Mask
AN-1238	Wide Bus Applications Using Parallel BLVDS SerDes Devices
White Paper	SerDes Architectures and Applications
DriveCable02EVK	DS15BA101/EA101Cable Driver/Equalizer Reference Design for 100+m Cable Driving
Reference Design	Redundant 18-bit SerDes Reference Design
Software	IBIS and BSDL Models
Serial Digital Interface (SDI)	
Design Guide	Broadcast Video Owner's Manual
Web Seminar	National's Solutions for HDTV Serial System Design
Web Seminar	Built-In SDV Test Pattern Generation Improves Video System Testing
Web Seminar	Obtaining Top Performance from National's SDI Cable Drivers and Equalizers
Reference Design	Low Cost 143-360 Mbps SDI Router Reference Design
FAQs	SDI/SDV Frequently Asked Questions (FAQs)
AN-1113	Serial Digital Video and Interface RAPIDESIGNER
AN-1320	Enhancing LMH0031 Jitter Performance With Easy-To-Use VCXOs
AN-1372	LMH0034 PCB Layout Techniques

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