Chapter 4

Noise Cancellation Techniques

4.1 Introduction

As with any other real world implementation of an experiment comes the ubiquitous noise which completely undermines nearly everything one originally plans in the design stages; our experiment was no exception. It could, in fact, be stated that noise, which by definition is any unwanted signal in one's electronics, was the number one issue plaguing this experiment from our original designs through completion.

By its very nature, this project specifically contains several key issues that defy common noise-cancellation techniques. What these issues are along with a brief synopsis of the common noise-cancellation techniques will be discussed.

Several noise cancellation techniques were utilized in this experiment and because of their profound consequences warrant their own chapter: the first of these is the build-in radiation protection of the VFAT2, charge-discriminating ICs, namely the Single Event Upset (SEU) triplicated logic and the Scan Chain ability for detecting erroneous digital gates; secondly, and also built into the VFAT2 controllers, are several differential-type signals that extend beyond the VFAT Breakout Board that the ISU LDS team designed; thirdly, the VFAT Breakout Board itself employs several noise cancellation techniques in its design and layout, many of which seem to defy common sense; also, the shielding and grounding techniques applied to the experiment as a whole along with their respective caveats and explanations; lastly are the design and implementation of S-Curves for setting the appropriate threshold levels of the VFATs to mitigate spurious signals even after all of the aforementioned noise-cancellation techniques are utilized.

4.2 Project-Specific Noise

4.3 Radiation Environment and Inability to Use Active-Network Noise Cancellation Techniques

The Region 1 detector is to be installed in a high-radiation environment; the normal usage of active-network noise cancellation techniques was therefore prohibited. Using active-networks, e.g. the usage of regular analog integrated circuits such as operational amplifiers, to effectively mitigate the noise was simply not possible because of their poor characteristics in a radiation rich environment with regards to both the added uncorrelated voltages and the permanent damage to their physical structure. This damage, even if it does not completely destroy the operation of the IC, can cause permanent shifts in operational amplifiers such as offset currents and voltages which may cause just as much noise in the circuit as one would hope to get rid of in the first place.

This, therefore, makes the design of the Region 1 detector all the more difficult. Designs such as Noise Shaping and Active Guard Drive were simply not feasible for this project. [8] Other techniques such as passive filtering, shielding, and special design techniques in the layout were employed by default and necessity.

4.3.1 GEM Trigger Pulse

The trigger pulse from the last stage of the GEM HV distribution network (see Figure 4-1) can be used to signify a hit on the detector. A hit on the detector releases a fairly consistent Gaussian-like pulse with a full-width-half-max (FWHM) of approximately 100ns from Trig Out. From a noise perspective it is useful to determine what the frequency content is of this pulse since one could then use this information to determine how much of the frequency energy content is from an actual hit and how much energy is from the noise and what frequencies the noise may contain.

It is known that the FWHM has the following relationship to the standard deviation, σ, of the Gaussian pulse:

$$\mathrm{FWHM} = 2\sqrt{2\ln 2}\,\sigma$$

Furthermore, the frequency content for a Gaussian pulse can be found using the Fourier Transform. For a Gaussian pulse this has the following form:

$$\mathcal{F}\{e^{-t^2/2\sigma^2}\} = \sigma\sqrt{2\pi}\, e^{-\sigma^2\omega^2/2}$$

As expected, as the FWHM of the time-domain pulse decrease, the FWHM of its respective Fourier Transform increase thereby causing the pulse to contain more high frequency content.

Using 100ns as the FWHM gives us: $\sigma = \frac{FWHM}{2\sqrt{2\ln 2}} = 42.466 \cdot 10^{-9}\, s$

The standard deviation in the frequency domain can then be found as the following:

$$\sigma_f = 1/\sqrt{4\pi^2\sigma^2} = 3.748\ MHz$$

Furthermore, since approximately 95% of the energy content is contained within two standard deviations of any Gaussian curve, any spectral content above double this frequency, namely 7.5 MHz, can be considered noise and is subject to removal via filtering.

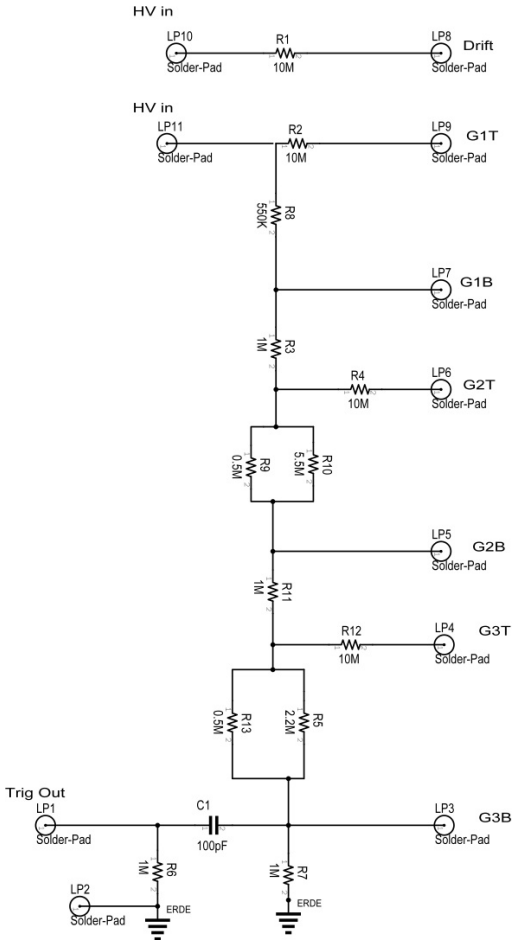

Figure 4-1: GEM HV Distribution Network

4.3.2 Frequency Dependent Noise

Since we often had coupling of the 40 MHz MCLK lines to the detector, it would be feasible to build a passive filter at the Trig Out site to filter out the energy content from the MCLK. A similar filter might have been used at the V1495 site of the ribbon cables between the VFAT Breakout Board and the V1495. The following pictures, show the Trig Out pulses both before and after a built-in 20MHz filter was applied on the signal by the oscilloscope. Because the filter is at the oscilloscope input, the noise from the MCLK is in reality still there.

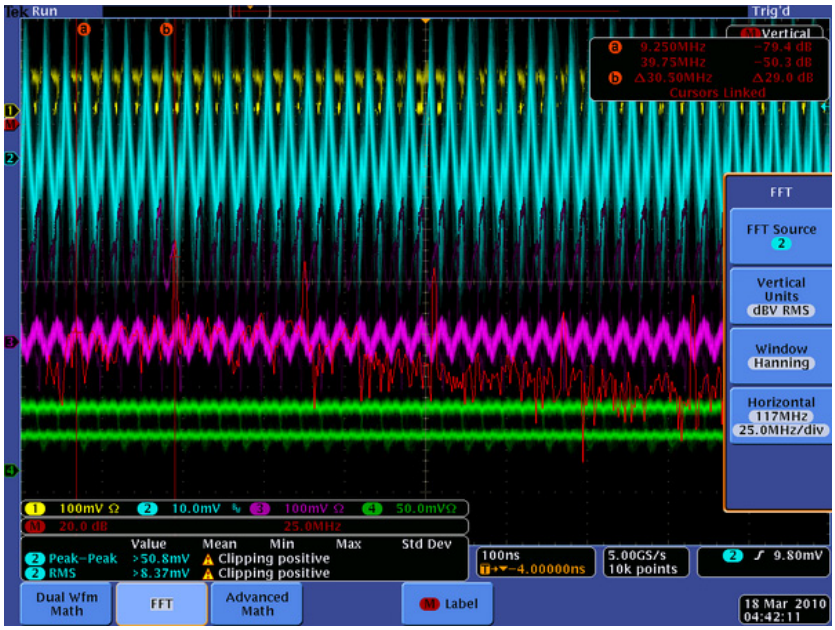

Figure 4-2: Unfiltered random signal on Trig Out with high level of cross-talk with MCLK

In Figure 4-2 above, the light-blue colored graph is the Trig Out signal with a very high level of noise. One can see from the red graph, the FFT of this signal, that there is an enormous out of energy at 40 MHz and it higher level harmonics, i.e. 80 MHz, 120 MHz. A hit signal on this line would be completely hidden and undetectable at this point.

With exactly the same setup, Figure 4-3 shows that applying a 20 MHz filter to the output of Trig Out actually lowers the noise from ~8.37 mV to ~1.37 mV. One can also see that the energy from the first harmonic of 40 MHz alone dropped 9dB and the other higher-order harmonics have all but disappeared at this point.

When a signal from Trig Out was captured on the oscilloscope as in Figure 4-4, the ~15 mV peak is easily discernible from the remaining noise. Also note that the extra energy from the pulse seems to be of a Gaussian shape and lie mostly below 10 MHz. This is in agreement to the energy calculations in the previous section if one were to adjust for a this particular pulse having a FWHM of ~80ns rather than 100ns.

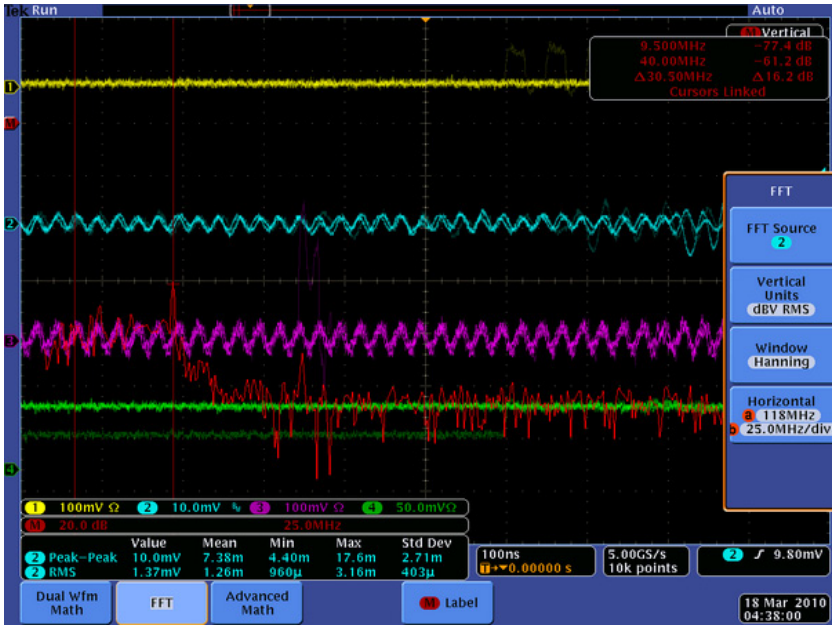

Figure 4-3: 20 MHz filter applied to random signal on Trig Out

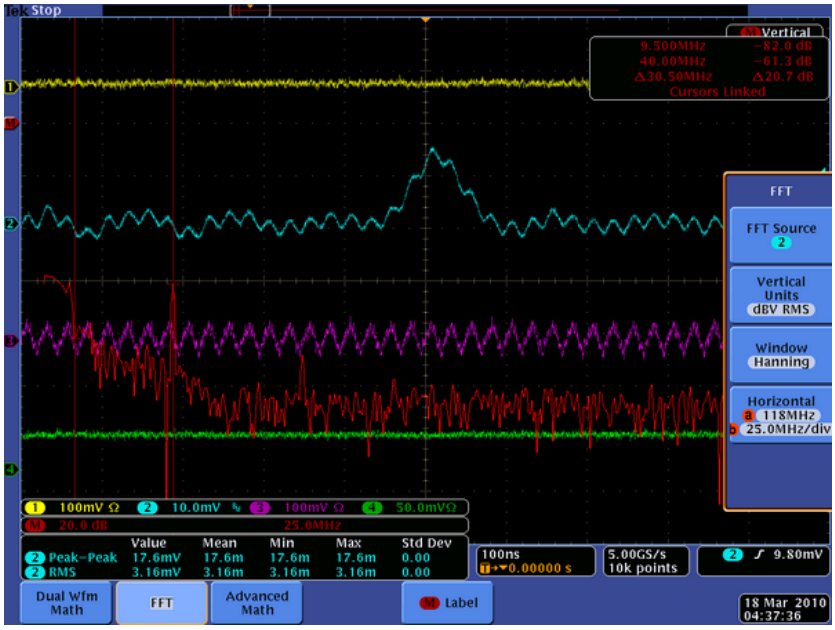

Figure 4-4: 20 MHz filter applied to actual hit signal on Trig Out with MCLK

In the end, it was found that using ungrounded shielding on both the ribbon cables to the VFAT cards themselves and the twisted-pair cables between the VFAT Breakout Board and the V1495 was more than effect enough to pull the RMS noise voltage on Trig Out to ~5 mV. (see “4.7 Shielding and Grounding”) At this level, the Trig Out pulse with an amplitude of ~10-20 mV should readily be detected.

4.3.3 Thermal Noise of the GEM High-voltage Distribution Network

Having familiarity with thermal noise and then observing a circuit built for DC high voltage with large resistors can cause a justified uneasiness. The easiest way to explain this is to first explain how thermal noise in a circuit is represented. Perhaps the most common way for representing quantifiable noise in general, $x_n(t)$, is by its root-mean-square (rms) value.

$$X_n = \left(\frac{1}{T} \int_0^T x_n^2(t) \right)^{1/2}$$

This rms value can be interpreted as the amount of power that the signal would consume if placed across a 1-Ω resistor.

Furthermore, it is commonly known that given multiple sources of noise, e.g. $x_{n1}(t)$, $x_{n2}(t)$, ... , that their summation can be determined as follows:

$$X_n^2 = \frac{1}{T} \int_0^T [x_{n1}(t) + x_{n2}(t)]^2 = X_{n1}^2 + X_{n2}^2 + \frac{2}{T} \int_0^T x_{n1}(t) x_{n2}(t)\, dt$$

And if the two signals are uncorrelated, the average of their product disappears, and the rms values add up as the square-root of the sum of the squares:

$$X_n = \sqrt{X_{n1}^2 + X_{n2}^2}$$

Thermal noise (a.k.a. Johnson-Nyquist Noise) is an inherent noise meaning that the noise is present simply due to the random fluctuations of the atoms in the composite material. In the case of resistors, the electrons themselves will move about in the material enough to cause measurable voltage/current fluctuation. These fluctuations which averaging out to zero (this is obvious or else there would be net positive power consumed or created) occur even if the resistor is sitting on a laboratory workbench completely disconnected from anything.

The power spectral density (or noise per unit frequency) for thermal noise is given as follows:

$$e_R^2 = 4kTR$$

Here e_R^2 can be taken as the power spectral density of a voltage source in series with a noiseless resistor.

Returning to the schematic of the GEM HV distribution network shown again in Figure 4-1, we see that on the voltage division side of the network there are several very high valued resistors each of these generating its own thermal noise.

For this analysis we ignore the effects of the GEM foil capacitors, and combine all of these resistances into one equivalent resistor. The result is the following:

$$e_{R_{eq}}^2 = e_{R8}^2 + e_{R3}^2 + e_{R9\|R10}^2 + e_{R11}^2 + e_{R5\|R13}^2 + e_{R7}^2$$
$$= 4kTR_{eq} = 1.65 \times 10^{-20}\, W/Hz \cdot 3.4157\ \text{M}\Omega$$
$$= 55.3 \times 10^{-14}\, V^2/Hz$$

This leaves us with the following equivalent circuit:

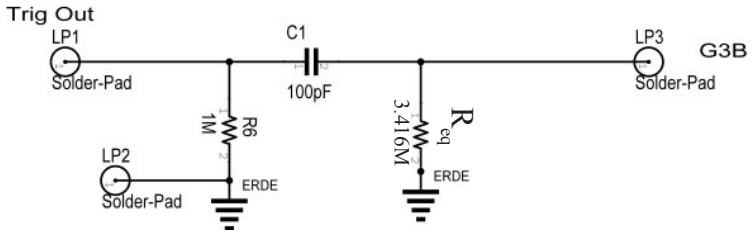

Figure 4-5: GEM HV Equivalent Noise Circuit

All we have remaining is to refer this noise to the Trig Out. It is also known that one can refer the noise spectrum, $S_{In}(f)$, through a linear time-invariant system with transfer function H(s) as follows:

$$S_{Out}(f) = S_{In}(f)\left|H(f)\right|^2$$

On the last leg of the HV Distribution network we have a simple highpass RC filter. This gives us the following relationship for the power spectral density of the noise referred to the GEM Trig Out:

$$S_{Out}(f) = S_{R_{eq}}(f)\left|\frac{V_{out}}{V_{R_{eq}}}(j\omega)\right|^2$$
$$= 4kTR_{eq}\frac{4\pi^2 R_6^2 C_1^2 f^2}{4\pi^2 R_6^2 C_1^2 f^2 + 1}$$

And since for our circuit, $(4\pi^2 R_6^2 C_1^2)^{-1/2} = 1592\ Hz$, this gives us a very low cutoff frequency for the high-pass filter of < 2 kHz. Therefore, for all intents and purposes, this highpass filter will filter out relatively little of the thermal noise generated by these resistors.

Lastly, we must simply integrate the total noise contribution in the valid field of measurement. From our frequency dependent noise discussion we can see the valid frequency range to be ~100 MHz. This gives us a total RMS voltage noise of $\sqrt{55.3 \cdot 10^{-14}\, V^2/Hz \cdot \sqrt{100\ MHz}} \approx 1mV$. Thus, we cannot hope to see the Trig Out signal is it drops below this value. Fortunately, we see that a typical Trig Out pulse has a peak value of ~15 mV.

4.4 VFAT2 Built-in Radiation Protection

The VFAT2 was created with the express purpose of operating in a radiation environment. In testing, the VFAT was able to withstand 10 Mrad of radiation with no observable effects[2]. Among other potentially built in features of the VFAT to ward against radiation effects, the VFAT offers two user accessible radiation protection features; the first of these is the Single Event Upset protection and the second is testing of digital gate through the Scan Path. With these features the VFAT is actually designed to withstand 100MRad of radiation.

4.4.1 Single Event Upset (SEU) Protection

The VFAT employs triplicated flip-flops in the Control Logic. If there is ever a discrepancy between the triplicated logic, a 2 to 1 "vote" is made by way of a logical "OR" of all of these outputs. The result is then used to increment an 8-bit synchronous counter. The result of this counter is then stored in an 8-bit register called the "UpsetReg". As with all of the registers on the VFAT, the I2C can then read back the values of this register. Of course, all of these details and can be found in the VFAT2 User Manual.[1]

4.4.2 Scan Path

As can also be read in the VFAT Manual, the Scan Path (a.k.a Scan Chain) enables testing of all of the logic flip flops. This is done by cascading all of the outputs of the flip flops rather than having them connected in their normal configuration. When put into "Scan Enable" mode, a serial pattern can be clocked into the VFAT via the ScanIn pin. After having passed through all of the available, cascaded flip flops the digital signal will then pass out of the ScanOut pin. The ScanClk pin is the same as the LVDS MCLK pin.

If all of the flip flops are operational then the two patterns will match with the exception of the signal being inverted. If, for instance, one of the flip flops is stuck high or low, the Scan Chain will read completely high or completely low respectively. If one or more of the flip flops are stuck at a fault, the VFAT chip may still be operational, but this will effectively count the "UpsetReg" once per fault per clock cycle. If more than one flip flop is stuck high or low then one would only be able to detect it by counting the change in the UpSetReg and then dividing by the number of MCLK periods that have transpired.

Implementation

Our own implementations of the Scan Chain are shown in the figures below. In Figure 4-7 a binary pseudo random bit sequence (PRBS) with base 8 is injected into the ScanIn of a single VFAT; the output can then be seen, Figure 4-8, on the ScanOut pin of the same VFAT.

For some reason unknown to the author, the bit pattern is actually inverted when passed through a single VFAT. At first it was believed that this was a simple polarity mistake in the setup. However, as demonstrated by directly daisy-chaining two VFATs on our VFAT Breakout Board inFigure 4-9, using the exact same setup (with the except of the daisy-chained VFATs), the signal again had the proper polarity as can be seen in Figure 4-10.

4.5 Differential-mode vs. Common-mode Signals

Basic lumped circuit theory relies on the assumption that the current carried in any transmission line is of equal and opposite polarity. This conforms to the "laws" of electromagnetics as well as making intuitive sense based on a closed-circuit model and Kirchhoff's Current Law (or more fundamentally the Conservation of Charge equation). Even more misleading is that in basic microwave theory the "bottom" conductor is referred to as "ground" and all voltages are referred to the "upper" conductor. The basic deficiency in this model is the closed-circuit portion of it. (I will not attempt to disprove the Conservation of Charge equation.)

Two fixes are proposed in *Introduction to Electromagnetic Compatibility* by Clayton Paul.[9] In either case, the first thing one needs to do is allow current to flow outside of the transmission line via conductivity or radiation. This allows for unbalancing the two different currents of the two conducting paths of the transmission line. The currents that travel in the equal and opposite direction are referred to as the differential-mode currents. The currents that travel in the equal but same direction as referred to as the common-mode currents. Obviously, some other transmission medium must be present (although not necessarily accounted for in this model) or else the circuit could not form a closed path.

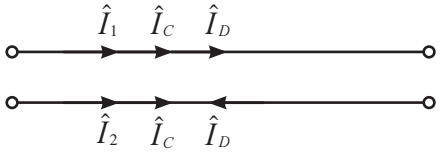

Figure 4-6: Common graphical depiction of differential-mode and common-mode current on a two-wire transmission line.

Figure 4-6 above shows graphically how the "upper" current and "lower" current both contribute to the total current. Mathematically these can be calculated as the following:

$$\hat{I}_1 = \hat{I}_C + \hat{I}_D$$
$$\hat{I}_2 = \hat{I}_C - \hat{I}_D$$

Figure 4-7: Single VFAT ScanIn PBRS with base 8 bit patter

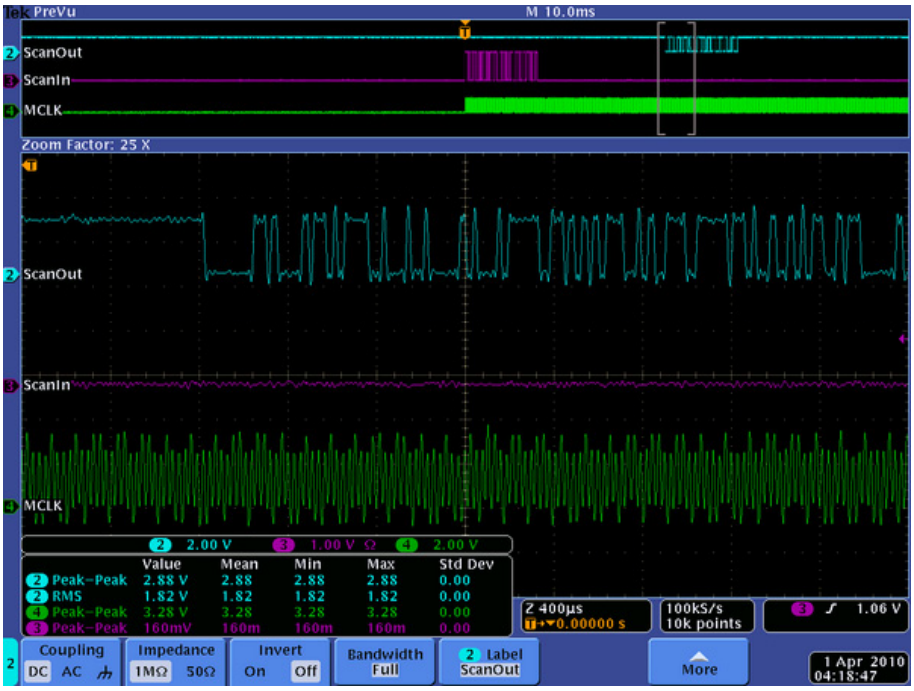

Figure 4-8: Single VFAT ScanOu

Figure 4-9: Daisy-Chained VFATs ScanIn bit patter

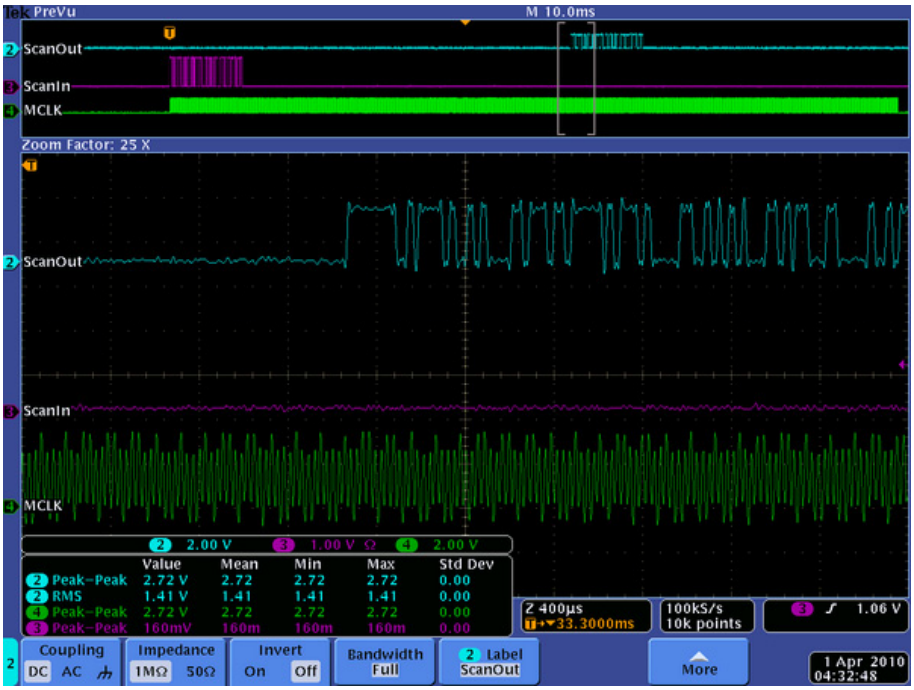

Figure 4-10: Daisy-Chained VFATs ScanOut bit patter

A simple algebraic manipulation of these equations in terms of the common-mode current and the differential-mode current yields the following:

$$\hat{I}_D = \frac{1}{2}(\hat{I}_1 - \hat{I}_2)$$
$$\hat{I}_C = \frac{1}{2}(\hat{I}_1 + \hat{I}_2)$$

At this point there is nothing to suggest that this makes any substantial difference in how we analyze the circuit. However, as can easily be demonstrated, the radiative electric fields due to each differential-mode current are nearly equal and opposite. Because these currents are of equal value, if it weren't for the slight difference in distance to the measurement location these electric fields would cancel, but instead there is a slight net electric field. The electric fields due to the common-more currents, however, actually add due to their being driven in the same direction. It is for this reason that radiated electric fields from common-mode currents are by far the predominant mechanism for producing radiated electric fields. In "4.7 Shielding and Grounding", we discuss how this effected our detector design and how we were able to resolve the problem.

4.6 VFAT Breakout Board Design

For this project we went through several designs for the VFAT Breakout Board. Each design added functionality and noise suppression. The number one problem with circuit board design and Electromagnetic Compliance (EMC) in general is the nasty habit of electrons to not read schematics.[9] In this section, we will discuss the various features of the VFAT Breakout Board.

4.6.1 Status Indicator LEDs

There are three differently colored LEDs on the VFAT Breakout Board that indicate different statuses of the board. The green LED is simply designed to indicated that there is sufficient power to the breakout board. If the voltage supply drops below 2 V, the green LED will only glow very dimly. Any lower than this and the LED will turn off. Care must be taken not to increase the voltage on the board beyond 3 V. Besides being much higher than the 2.75 V rating of the VFATs, this voltage is likely to damage the green LED as it will begin to draw too much current.

The yellow and red status LEDs indicate a Status problem or Error. These LEDs can only be set by the I^2C Expander chip and are software controlled by the Gumstix controller. The yellow or red LED is turned on by writing a 0 to bit 7 or bit 6 (0x7F or 0xCF) to the I^2C Expander respectively. The bit lines run from 0 - 7, as is common for many electronics.

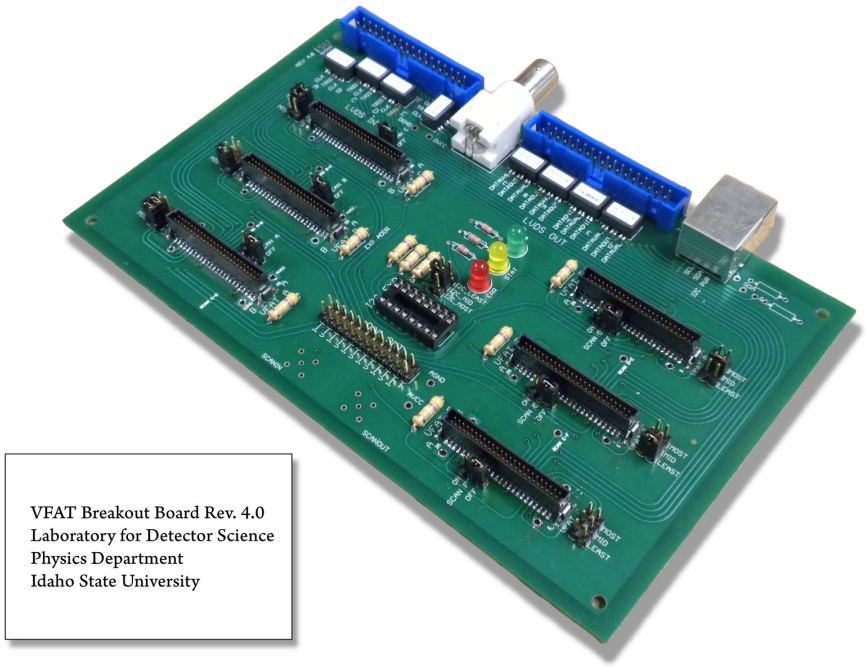

Figure 4-11

4.6.2 I²C Address and Scan Enable Jumpers

Each of the binary I²C addresses of the six ports on the VFAT Breakout Board are completely selectable via the jumpers physically next to that port. Each of these jumpers contain the top three MSBs of a seven-bit I²C address and are labeled “MOST”, “MID”, and “LEAST”. One can therefore select any of six address from 0x16 - 0x112 by multiples of 16. By convension the port numbers are assigned in ascending order from 0x16 through 0x112 skipping over 0x32 because this is the default address of the on-board I²C expanded (located in the center of the board) if it is utilized. These are the addresses of the VFAT Ports A through F respectively. Jumping a pin will connect that respective address pin to ground thereby signifying a 0. If the jumper is not connected then internal pull-up resistors inside of the VFATs will pull the address line high thereby signifying a 1. For example to get the I²C address 0x16 one would jump the first two MSBs and leave the LSB floating. For the I²C address 0x112 one would leave all of the I²C address lines floating thereby leaving all three bits high.

The only exception to this are the address pins to the I²C Expander; these are set in the reverse fashion as the VFATs. Each address pin is jumped with it is to be set high, e.g. 1, and left floating for a low, e.g. 0.

The Scan Enable pins must be jumped either high or low. To enable the Scan Chain functionality of the VFATs one must jump the ScanEn pin high (as is properly indicated by the silk screen on the board). Otherwise, one must jump this pin low. Failure to do so will cause the VFAT chips to operate improperly.

4.6.3 Soft Reset

The Soft Reset pins to the VFATs are all active low. These are software controlled via the I2C expander. To reset a VFAT using a Soft Reset one must send a logic 0 to that respective VFAT by writing a 0 on bit line 0 - 5 for VFAT A - F respectively. Furthermore, since these Soft Reset lines are connected with pull-up resistors, these lines will all pull to VCC when an I^2C Expander chip is not present.

4.6.4 Common-mode Chokes

Revision 4.0 of the VFAT Breakout Board includes common-mode chokes on all of the LVDS signals both entering and exiting the board. See Figure 4-12. The purpose of these chokes is to mitigate the spurious common-mode signals on the ribbon cables between the VFAT Breakout Boards and the V1495. As explained in “4.5 Differential-mode vs. Common-mode Signals“, these signals arise due to a difference in ground potential between the two different systems and cause radiative coupling to other components much more readily than differential signals. Also, to see how we circumvented these radiative current see ““.

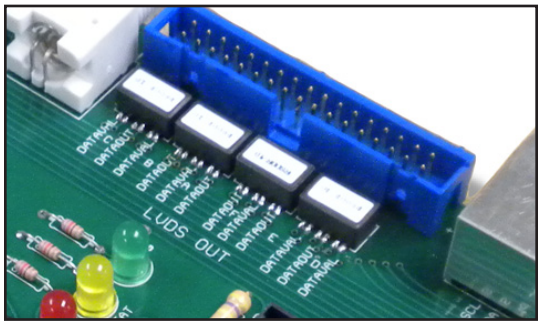

Figure 4-12: Common-mode chokes on DataVal and DataOut

These chokes are wire pairs wrapped in opposite directions about the same toroidal ferromagnetic core. Ideally this allows the differential signals to pass through completely unabated but any common-mode signals will find these coils to provide a very high impedance as the mutual inductances of the two different loops completely cancel each other out. Section “5.9 Common-mode Chokes” and “Chapter 9 Crosstalk” in *Introduction to Electromagnetic Compatibility*[9] give an excellent discussion on this subject. Figure 4-13, which can be found

in the aforementioned book, illustrates a basic sketch of this toroidal configuration used to block common-mode currents.

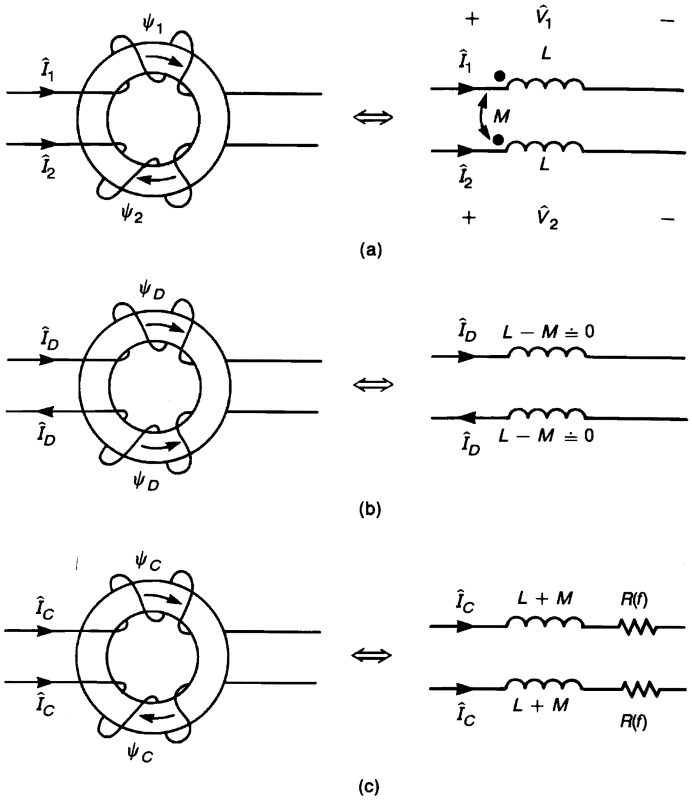

Figure 4-13: (a) the currents of a two-wire line, (b) the differential-mode components, and (c) the common-mode components

4.6.5 Minimizing Current Loops

Undoubtably one of the most important improvements made on Rev 4.0 of the VFAT Breakout Board is the reduction of current loops. This is perhaps the only aspect of this circuit board that can explain why several of our ports failed to communicate via LVDS signals on previous versions of the board; no other single aspect can explain this since the electrical connects of the other boards are identical and we used the exact same cables as before.

It can be shown that as the loop area of a current path increases, the total impedance due to inductance increases as well. This comes as the difference between the inherent self inductance becomes much greater compared to the mutual inductances; the mutual inductances actually acts to decrease the voltage drop due to total inductance in a conductor.[9] In particular, it is extremely important to reduce the amount of voltage drop through the power and ground planes, otherwise the supply voltage ripple can filter through to both the analog and digital

functionality of the components; even the ones that are not necessary responsible for creating the voltage supply ripple.

This also manifests itself in two other common ways:

The first is when there is a break in the power or ground plane supplying the current. This break forces the current to divert itself around the break thereby increasing the current loop and once again increasing the current loop and inductance. Every effort has been made to not break the ground or power planes in line with the regular currents needed by the VFATs or other components. There are very few instances where is was necessary to use a small portion of the power and/or ground planes for a regular signal, but these mainly towards the side farthest from the power supply.

Second, it is a commonly-held misconception that the digital and analog power planes should be electrically separated. While it is true that the two segments should physically be located in different regions of the board, it is not better to actually separate the two planes. [10],[11] There are several reasons for this, the least of which is if currents travel from the digital power supply over to the analog ground or vica versa, the current loops from these can be tremendous.

4.6.6 Geographical Layout of Components

Besides using solid power and ground planes our latest version of the VFAT Breakout Board uses judicious geographical placement of the various components. The basic rules to obey for this are very basic: the highest frequency components should be as far away from the power supply of the board as possible and as the speed decreases and the precision of the voltage values increases (as in the case of the analog components), the components must be physically placed closer to the power supply.

There are two basic reasons for this layout: first, the longer the land distances between the high-speed components and the power supply, the more they will take advantage of the impedances already inherent to the board thereby lessening the effects of there higher harmonics; second, the longer the conductor distance that two currents from two different sources share together, the more that they will share common voltage drops due to common-impedance coupling. Thus, the longer one runs a sensitive signal along the same current path with a high-speed signal, the more likely it is for the sensitive signal to couple with the high speed signal and become distorted.[9] Figure 4-14 below shows the layout file of the VFAT Breakout Board Rev. 4.0 and the respective locations of the different types of signals with regards to their signals.

Lastly, one must as much as possible place the off-board connectors on the same side of the board. Failure to do so can set up oscillating signals across the power planes that can cause an

inordinate amount of radiation.[9] So while it makes the layout much easier to place off-board connectors on different sides of the board, this must be avoided if at all possible. The only exception to this are the DAC outputs and the Scan Chain I/Os. In this case, these signals will only be utilized when most of the other LVDS signals are dormant.

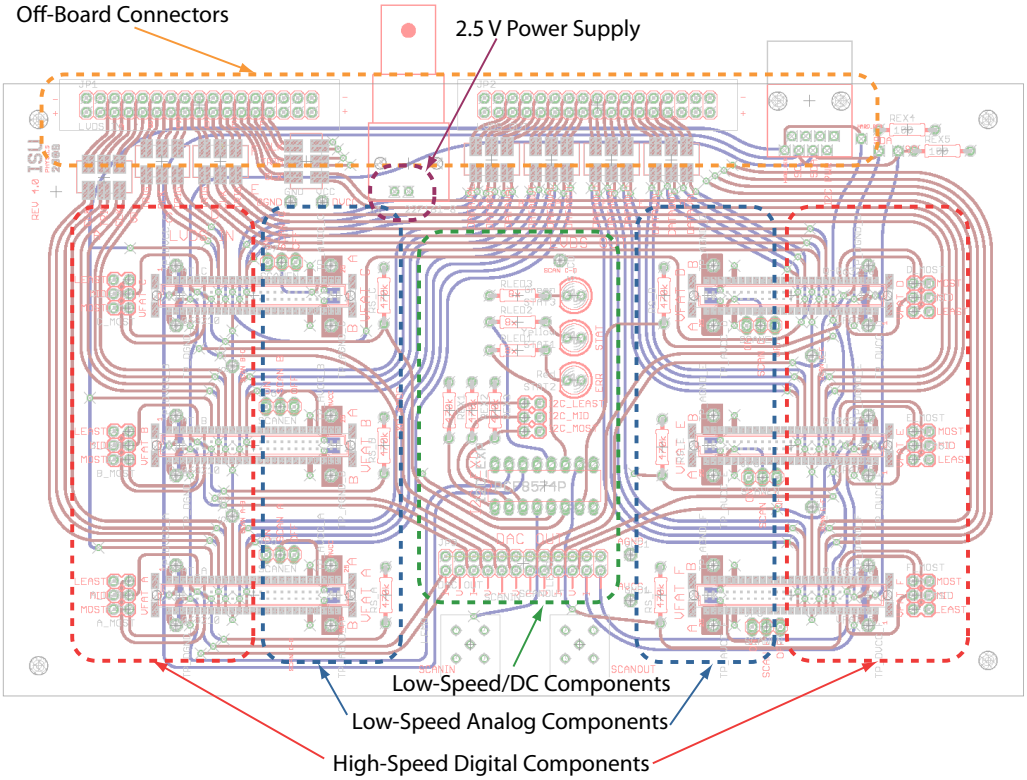

Figure 4-14: VFAT Breakout Board layout with specific regions based on speed emphasized

4.7 Shielding and Grounding

4.7.1 Implementation

As previously discussed, we ultimately found that the last remaining noise cancellation technique that was necessary to employ was shielding of both our VFAT ribbon cables as well as our by either tinfoil (as in the case of the VFAT ribbon cables) or ungrounded mesh clading on twisted pair cable. As a quick side note; it was found earlier that ungrounded shielded cable

without twisted pairs caused two of our VFAT cards to quit transmitting properly.

For our latest HRRL and cosmic particle experiments we implemented this configuration, and it proved to be quite effective. In Figure 4-15 below, we can see our setup for the HRRL experiment. Emphasis has been added to where the shielded cables are located for reference in this discussion.

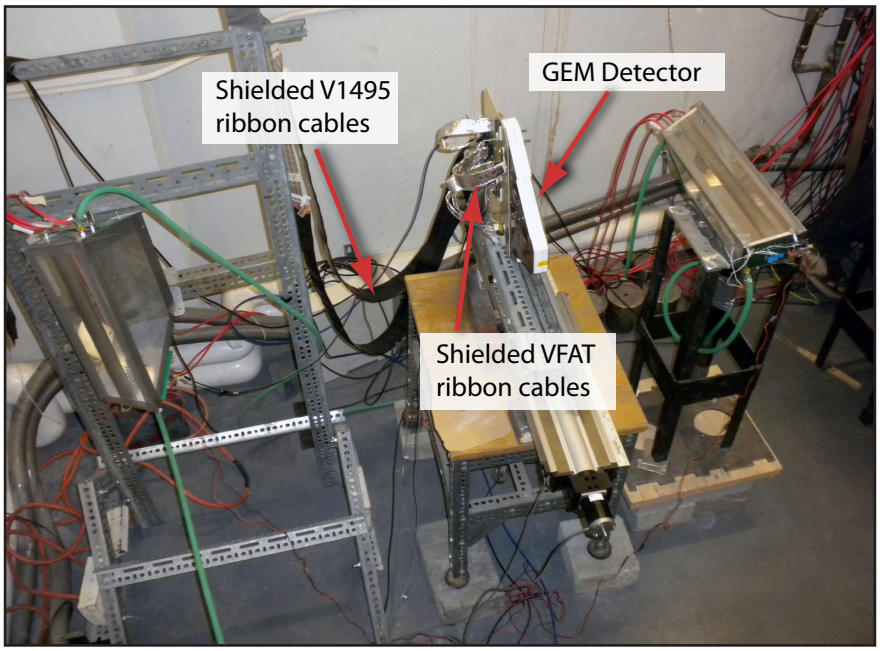

Figure 4-15: HRRL Experiment Setup

4.7.2 Explanation

Despite the fact that there are common-mode current chokes on the inputs and outputs of the VFAT Breakout Board, there can still be common-mode voltage on the lines. In other words, just because there is a high impedance to common-mode sources does not mean that the voltage goes away. In fact, it can be quite the opposite. Not having common-mode current can actually raise the voltage because there is no longer any voltage drop from the common-mode source impedance. By essentially attempting to eliminate the common-mode current we actually raised the common-mode voltage on the line. This is all the more pronounced because have low-resistance, 50-Ω cables. Having raised the common-mode voltage actually means that we will have a higher propensity for capacitive coupling to other parts of the system.

Both the shielding for the VFAT ribbon cables as well as the V1495 ribbon cables successfully employ the same basic technique to drastically reduce the coupled voltage to the GEM Detector-- surround the ribbon cable with an ungrounded metallic shield. There are a number of reasons why this would at first glace appear to defy common sense.

First, due to the speed of the signal and the proximity of the components, these fields are primarily static electric fields causes by a change in common-mode voltage on the respective cables. Gauss' Law states that the total charged contained within any Gaussian surface can be determined by the integration of the total electric flux found at that surface. Without any insulators present there is nothing to block the electric fields from leaving the shielding as if there were nothing there at all.

Looking at this more quantitatively we can find the answer. We can use the multiconductor transmission-line (MTL) model as proposed by Clayton Paul in *Introduction to Electromagnetic Compatibility* with a slight variation.[9] There in section 9.7.2 pg. 651 he proposes the following four-conductor model as shown below in Figure 4-16.

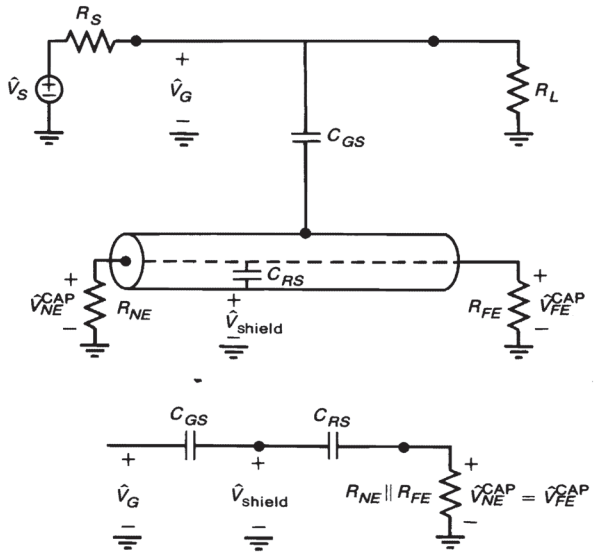

Figure 4-16: Four-wire model to demonstrate effects of shielding

Here he has shown the signal from the unshielded wire capacitively coupling to the signal wire inside of the shield. In our experiment we are interested in shielding the wires containing the signals and thereby protecting the detector from coupling capacitively to the signals wires. We can simply exchange the source voltage and exchange all of the impedances as shown in Figure 4-17. Note how the equivalent circuit does not change. This makes the math exactly the same for our purposes:

$$\hat{V}_{NE}^{CAP} = \hat{V}_{FE}^{CAP} = \frac{j\omega RC_{RS} \parallel C_{GS}}{1 + j\omega RC_{RS} \parallel C_{GS}} \hat{V}_G$$

where

$$R = \frac{R_{NE}R_{FE}}{R_{NE} + R_{FE}}$$

$$C_{RS} \parallel C_{GS} = \frac{C_{RS}C_{GS}}{C_{RS} + C_{GS}}$$

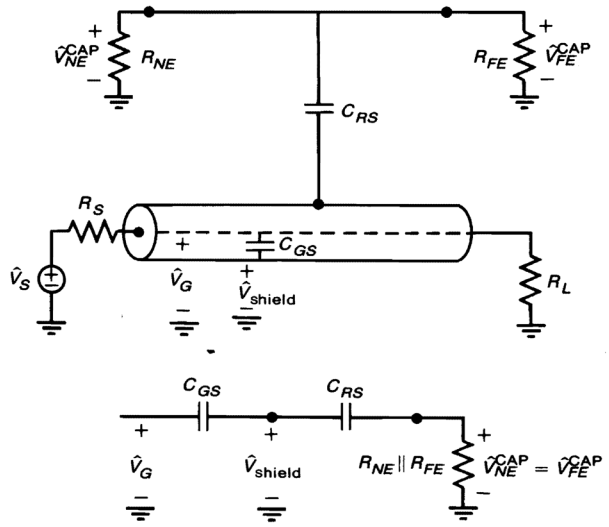

Figure 4-17: Four-wire model modified for the Detector 1 shielding

This coupling equation is nothing more than another high-pass filter. Frequencies below the cutoff frequency of $(2\pi RC_{RS} \parallel C_{GS})^{-1}$ will be attenuated but frequencies above this are passed through completely. Furthermore, decreasing the equivalent capacitance will push the cutoff frequency higher and attenuate the coupled signal more.

What can also be said for this model is that capacitors add in series just like resistors in parallel. That is to say that the lowest capacitor (particularly if it much lower than the other) will dominate the equivalent capacitance. Normally, $C_{RS} \gg C_{GS}$ which would imply that $C_{RS} \parallel C_{GS} \cong C_{GS} \cong C_{GR}$. This basically means that for a capacitive system where the line couples more strongly to the shield than to the external system it is as if the shielding is not even there. This seems to confirm what was intuitively discovered from the argument based on Gauss' Law. And yet the shielding works; what is going on here?

There can be only one answer; as long as there are no egregious errors in this model then it must be that the capacitance from the signal wires to the shield couples much *less* strongly than the shield to the GEM detector or even the signal wires to the GEM detector, e.g. $C_{RS} \ll C_{GS}$. This is a rare case, but it also makes sense. Despite the fact that the shield is a metal casing completely surrounding the signals wires at a very short distance (all the necessary components of a strong capacitor), the GEM detector itself is a series of large -- respectively speaking -- copper plates. Apparently this combination of copper plates on the GEM detector makes for a larger capacitor than the shielding wrapped around the signal wires.

Normally, the only way to get this kind of effect is to provide a solid ground connections at points 0.1λ, e.g.10% of the electrical wavelength, to provide a grounding potential on the shielding cable. This assures that no voltage can couple to the shield thereby protecting the external circuits from the signal wire.

4.8 VFAT Channel Calibration via S-Curves

4.8.1 Implemenation

4.8.2 CalPulse Implemenation