GEM Readout Controller Firmware Status

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1. GEMReadout Firmware Revision 1.0 completed for CAEN V1495 Module
   - Utilizes ~25% of logic resources and ~70% of block RAM on user FPGA
   - Meets 32MHz target clock with plenty of slack

2. GEMReadoutCtrl VxWorks readout routines completed
   - VME event data readout done without DMA (this reduces performance by about a factor 4, if DMA is used then a 20kHz trigger rate is easily achieved)
   - 12 GEM DATA/DATAVALID streams pumped into the V1495 and read out at 5kHz (after continuous >5.4kHz rate, events are lost – limiting factor VME readout method).

   Sample 192bit Frame sent to 12 GEM channel inputs (LSW on the left):

   A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC

   N Status events were reported by the GEMReadoutCtrl indicating GEM channel statistics. The following definitions are for the output symbols using in the Test Code Output:

   GEM[a]: #B[b] #F[c/d] B/s[e] F/s[f] LstEvtCnt[g] LstWrdCnt[h]

   Lower case letters a-h in the above statement are defined as follows:
   a – GEM Channel# (0-11)
   b – Total Bytes Read from GEM Channel
   c – Total Frames Readout from GEM Channel
   d – Total Frames sent from GEM module (d-c would be #frames dropped)
   e – VME bytes per second read from GEM Channel
   f – Frames per second from GEM Channel (trigger rate)
   g – Last read event count for GEM channel (events are lost when 63 is reached)
   h – Last event word count for GEM channel

   Yellow Event Status Update #N-2 (5.4kHz Trigger Rate)
   Each GEM(0-11) reports a trigger rate of 5.4kHz each channel utilizing 129,720 bytes per second of the VME backplane (cumulative ~1.5MByte/sec). Event buffer contains ~10 events. Read event counts don't match the V1495 received GEM frame counts since readout is ongoing.

   Green Event Status Update #N-1 (Trigger Shut Off)

Remaining buffered events are readout.

Cyan Event Status Update #N (Readout Completed)

Event readout complete. Each GEM channel reported receiving 70,907 frames, which matches exactly what has been read out indicating no frames have been dropped. Going beyond 5.4kHz average trigger rate will lose events.

Test Code Ouput:

```
GEM[0]: #B[1692696] #F[70529/70547] B/s[129720] F/s[5405] LstEvtCnt[17] LstWrdCnt[216]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[1]: #B[1692696] #F[70529/70548] B/s[129720] F/s[5405] LstEvtCnt[13] LstWrdCnt[216]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[2]: #B[1692696] #F[70529/70550] B/s[129720] F/s[5405] LstEvtCnt[13] LstWrdCnt[216]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[3]: #B[1692696] #F[70529/70551] B/s[129720] F/s[5405] LstEvtCnt[5] LstWrdCnt[216]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[4]: #B[1692696] #F[70529/70553] B/s[129720] F/s[5405] LstEvtCnt[17] LstWrdCnt[216]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[5]: #B[1692696] #F[70529/70554] B/s[129720] F/s[5405] LstEvtCnt[10] LstWrdCnt[216]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[6]: #B[1692696] #F[70529/70555] B/s[129720] F/s[5405] LstEvtCnt[13] LstWrdCnt[216]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[7]: #B[1692696] #F[70529/70557] B/s[129720] F/s[5405] LstEvtCnt[2] LstWrdCnt[216]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[8]: #B[1692720] #F[70530/70558] B/s[129720] F/s[5405] LstEvtCnt[8] LstWrdCnt[216]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[9]: #B[1692720] #F[70530/70561] B/s[129720] F/s[5405] LstEvtCnt[4] LstWrdCnt[216]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[10]: #B[1692720] #F[70530/70562] B/s[129720] F/s[5405] LstEvtCnt[15] LstWrdCnt[216]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[11]: #B[1692720] #F[70530/70564] B/s[129720] F/s[5405] LstEvtCnt[6] LstWrdCnt[216]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[0]: #B[1701768] #F[70907/70907] B/s[9072] F/s[378] LstEvtCnt[0] LstWrdCnt[0]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[1]: #B[1701768] #F[70907/70907] B/s[9072] F/s[378] LstEvtCnt[0] LstWrdCnt[0]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[2]: #B[1701768] #F[70907/70907] B/s[9072] F/s[378] LstEvtCnt[0] LstWrdCnt[0]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[3]: #B[1701768] #F[70907/70907] B/s[9072] F/s[378] LstEvtCnt[0] LstWrdCnt[0]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[4]: #B[1701768] #F[70907/70907] B/s[9072] F/s[378] LstEvtCnt[0] LstWrdCnt[0]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[5]: #B[1701768] #F[70907/70907] B/s[9072] F/s[378] LstEvtCnt[0] LstWrdCnt[0]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[6]: #B[1701768] #F[70907/70907] B/s[9072] F/s[378] LstEvtCnt[0] LstWrdCnt[0]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[7]: #B[1701768] #F[70907/70907] B/s[9072] F/s[378] LstEvtCnt[0] LstWrdCnt[0]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[8]: #B[1701768] #F[70907/70907] B/s[9048] F/s[377] LstEvtCnt[0] LstWrdCnt[0]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[9]: #B[1701768] #F[70907/70907] B/s[9048] F/s[377] LstEvtCnt[0] LstWrdCnt[0]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[10]: #B[1701768] #F[70907/70907] B/s[9048] F/s[377] LstEvtCnt[0] LstWrdCnt[0]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[11]: #B[1701768] #F[70907/70907] B/s[9048] F/s[377] LstEvtCnt[0] LstWrdCnt[0]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[0]: #B[1701768] #F[70907/70907] B/s[0] F/s[0] LstEvtCnt[0] LstWrdCnt[0]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[1]: #B[1701768] #F[70907/70907] B/s[0] F/s[0] LstEvtCnt[0] LstWrdCnt[0]
  LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
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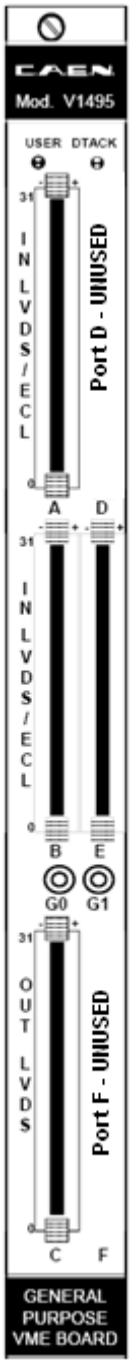
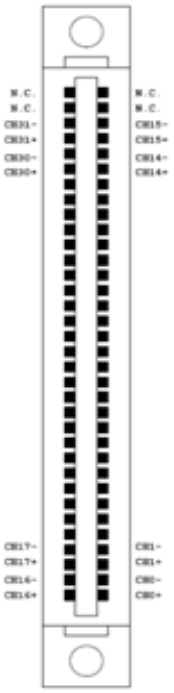
GEM[2]: #B[1701768] #F[70907/70907] B/s[0] F/s[0] LstEvtCnt[0] LstWrdCnt[0]
LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[3]: #B[1701768] #F[70907/70907] B/s[0] F/s[0] LstEvtCnt[0] LstWrdCnt[0]
LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[4]: #B[1701768] #F[70907/70907] B/s[0] F/s[0] LstEvtCnt[0] LstWrdCnt[0]
LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[5]: #B[1701768] #F[70907/70907] B/s[0] F/s[0] LstEvtCnt[0] LstWrdCnt[0]
LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[6]: #B[1701768] #F[70907/70907] B/s[0] F/s[0] LstEvtCnt[0] LstWrdCnt[0]
LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[7]: #B[1701768] #F[70907/70907] B/s[0] F/s[0] LstEvtCnt[0] LstWrdCnt[0]
LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[8]: #B[1701768] #F[70907/70907] B/s[0] F/s[0] LstEvtCnt[0] LstWrdCnt[0]
LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[9]: #B[1701768] #F[70907/70907] B/s[0] F/s[0] LstEvtCnt[0] LstWrdCnt[0]
LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[10]: #B[1701768] #F[70907/70907] B/s[0] F/s[0] LstEvtCnt[0] LstWrdCnt[0]
LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC
GEM[11]: #B[1701768] #F[70907/70907] B/s[0] F/s[0] LstEvtCnt[0] LstWrdCnt[0]
LastCap[12]: A012 C345 E678 9ABC DEF0 1234 5678 9ABC DEF0 1234 5678 9ABC

GEM Readout Controller Module Pinouts



32 Channel Input/Output Module Pinout



Ch	PortG
0	32MHZ CLK IN (NIM)
1	TRIGGER IN (NIM)

Ch	PortA	PortC	PortE (A395C)
0	GEM1A: DATA_VALID	T1	TEST_DATA_VALID
1	GEM1A: DATA	CLK	TEST_DATA
2	GEM1B: DATA_VALID	T1	TEST_DATA_VALID
3	GEM1B: DATA	CLK	TEST_DATA
4	GEM1C: DATA_VALID	T1	TEST_DATA_VALID
5	GEM1C: DATA	CLK	TEST_DATA
6	GEM1D: DATA_VALID	T1	TEST_DATA_VALID
7	GEM1D: DATA	CLK	TEST_DATA
8	GEM1E: DATA_VALID	T1	TEST_DATA_VALID
9	GEM1E: DATA	CLK	TEST_DATA
10	GEM1F: DATA_VALID	T1	TEST_DATA_VALID
11	GEM1F: DATA	CLK	TEST_DATA
12	Unused	Unused	Unused
13	Unused	Unused	Unused
14	Unused	Unused	Unused
15	Unused	Unused	Unused
16	GEM2A: DATA_VALID	T1	TEST_DATA_VALID
17	GEM2A: DATA	CLK	TEST_DATA
18	GEM2B: DATA_VALID	T1	TEST_DATA_VALID
19	GEM2B: DATA	CLK	TEST_DATA
20	GEM2C: DATA_VALID	T1	TEST_DATA_VALID
21	GEM2C: DATA	CLK	TEST_DATA
22	GEM2D: DATA_VALID	T1	TEST_DATA_VALID
23	GEM2D: DATA	CLK	TEST_DATA
24	GEM2E: DATA_VALID	T1	TEST_DATA_VALID
25	GEM2E: DATA	CLK	TEST_DATA
26	GEM2F: DATA_VALID	T1	TEST_DATA_VALID
27	GEM2F: DATA	CLK	TEST_DATA
28	Unused	Unused	Unused
29	Unused	Unused	Unused
30	Unused	Unused	Unused
31	Unused	Unused	Unused

Port A Description

PortA is a 32 channel LVDS input used to supply 12 GEM DATA/DATA_VALID streams into the CAEN1495 for capturing. These data signals are synchronous to the 32MHz CLK of the V1495. Setup/hold timing information has not yet been determined, this timing can be managed by varying the PortA -> GEM Breakout box cable length.

Port C Description

PortA is a 32 channel LVDS output used to supply 12 GEM CLK/T1 streams into the GEM Breakout boxes. These data signals are synchronous to the 32MHz clock of the V1495. T1 is launched from the rising edge of the internal V1495 clock, while CLK is launched from the negative edge of the internal clock. This is intended to provide a large setup/hold time for the GEM (the GEM should capture the T1 on the rising edge of the received CLK).

Port E Description

PortE is a 32 channel LVDS output used to supply 12 GEM DATA/DATA_VALID streams into the V1495 PortA for testing. These data signals are synchronous to the 32MHz clock of the V1495. Using a short loopback cable, <1 meter should be fine, (ensure that LVDS channel#1 PortE goes to channel#1 of PortA – you need an ugly twist in the cable to do this).

Port G Description

PortG is a 2 channel NIM input. G0 is the reference clock for the V1495 and GEM modules. This reference clock is multiplied by 1 using an internal PLL on the V1495, resulting in a 32MHz system clock for a 32MHz reference input. This PLL will lock on to a reference clock of 32MHz +/- several MHz. G1 is a NIM trigger input, that is synchronized to the reference clock internal to the V1495. The optimal setup/hold time can be found by looking at the T1 outputs of PortC while delaying the G1 input with respect to G0 (once you see the T1 output shift a clock cycle, add or remove half a clock period delay from the trigger input cable).

GEM Readout Controller Module Firmware Features

- Buffers 63 events (each event contains 12x 192bit data streams received in parallel from 12 GEM Modules)
- Drives 12x T1/CLK LVDS output signals for GEM modules
- Receives 12x DATA/DATA_VALID LVDS input signals from GEM modules
- NIM reference clock input
- NIM trigger input (synchronous to reference clock).

Event Buffering

The firmware implements a 63 deep event FIFO for all 12 GEM input channels, where each event holds up to a 192bit serial stream. An event count for each GEM channel is monitored to determine when an event is ready for readout. When a VME transaction indicates a non-zero event count, the event size for that GEM channel can be read from the EventSize FIFO. Under normal circumstances the event size should be 12, indicating 12x 16bit words for the GEM channel event (= 192 bits). Once the event size is known, the EventData FIFO can be readout. Since the V1495 does not support interrupts on the VME backplane the VME CPU must poll the V1495 event counters to determine when to begin readout.

The V1495 supports A24/A32 VME addressing modes (the VxWorks readout code implements A32 only, but is easily changed). The V1495 will only respond to D16 transactions. Current testing indicates a ~5kHz average trigger rate can be sustained with the current event buffer routines/mechanisms implemented.

T1/External Triggers

A hard and soft 3bit trigger word can be defined in the V1495 VME registers. The hard trigger word is sent serially out all T1 signals whenever a rising edge is detected on the NIM trigger input. The serial nature of the T1 encoding restricts trigger outputs from being generated if trigger input rising edges arrive closer than 3 clock cycles apart from each other.

A soft trigger word is sent serially out all T1 signals whenever the soft trigger VME register is written. If a hard trigger word is in the process of being shifted out the soft trigger will be ignored.

GEM Test Frame Generator

A 192bit serial frame can be defined through the VME registers which is used for testing the serial DATA/DATA_VALID input signals on PortA. This test frame can be sent out PortE, which emulates the 12 GEM outputs, and can sent directly into PortA using a straight through ribbon cable. This test frame can be sent by written the appropriate

VME register, or it can be setup to be sent when an external trigger is seen (ideal for testing).

GEM VME Firmware Registers

All VME registers are accessed through A32/A24 D16 accesses.

Access Types:
R/W – Readable and Writable RO – Read Only WO – Write Only

Register: **BoardID** Offset: **0x0000** Access Type: **RO**

Description: Contains CAEN 3bit board identifies for slots D, E, F.

000b A395A Module
001b A395B Module
010b A395C Module
011b A395D Module

Bits	Description
2:0	Board ID D
5:3	Board ID E
8:6	Board ID F
15:9	Unused

Register: **Revision** Offset: **0x0002** Access Type: **RO**

Description: Contains GEMReadout V1495 Firmware Revision

Bits	Description
7:0	Minor Revision
15:8	Major Revision

Register: **Reset** Offset: **0x0004** Access Type: **WO**

Description: Resets Module and registers to default settings

Bits	Description
15:0	don't care

Register: **GEMTxStart** Offset: **0x0010** Access Type: **WO**

Description: Generates a GEM Test frame out on PortE

Bits	Description
0	'1' generates 1 "soft" test frame trigger
1	'1'=Enable, '0'=Disable: External Trigger to generate test frame
15:2	don't care

Register: **GEMSoftTrig** Offset: **0x0012** Access Type: **WO**

Description: Generates a T1 trigger word (defined by SOFT trig word)

Bits	Description
15:0	don't care

Register: **GEMTrigWord** Offset: **0x0014** Access Type: **WO**

Description: Define the HARD and SOFT T1 trig words

Bits	Description
2:0	SOFT trig word definition
5:3	HARD trig word definition

Register: **GEMTxWord[B:0]** Offset: **0x0014-0x002D** Access Type: **WO**

Description: Define the 192bit GEM test frame. The first address location, MSB corresponds to the first bit shifted out.

Bits	Description
15:0	16bit WORD

Register: **GEMxy_FIFOSize[B:0]** Offset: **0x0030-0x0047** Access Type: **RO**

Description: Returns FIFO sizes indicating number of stored events and total event words. Address location corresponds to GEM channel number.

Bits	Description
5:0	Number of Buffered Events
15:6	Cumulative Event Data Size

Register: **GEMxy_EventSize[B:0]** Offset: **0x0048-0x005E** Access Type: **RO**

Description: Return the next event size (number of 16bit words) for the corresponding GEM channel. Address location corresponds to GEM channel number.

Bits	Description
3:0	Event Word Count
15:4	reserved

Register: **GEMxy_Events_Sent_H[B:0]** Offset: **0x0080-0x0096** Access Type: **RO**

Description: Upper 16bit word corresponding to the total number of events the corresponding GEM channel has ever transmitted (this counts whether or not the V1495 has room to buffer the event and allows a way to determine how many events have been lost). Reading this register automatically latches the lower 16bits of the value in a common holding register where it can be read by reading the _L part of this register.

Bits	Description
15:0	Total GEM Frames Sent bits 31:16

Register: **GEMxy_Events_Sent_L[B:0]** Offset: **0x00A0-0x00B6** Access Type: **RO**

Description: Lower 16bit word corresponding to the total number of events the corresponding GEM channel has ever transmitted (this counts whether or not the V1495 has room to buffer the event and allows a way to determine how many events have been lost). This register automatically latched after reading the _H part of this register.

Bits	Description
15:0	Total GEM Frames Sent bits 15:0

Register: **GEMxy_EventsData[B:0]** Offset: **0x4000-0x4BFF** Access Type: **RO**

Description: Contains the event data for each GEM channel. This memory is segmented into 256 portion, where the first segment is for GEM channel 0, the next for channel 1 and so on. The correct number of reads must be performed here or the FIFO will be out of sync. The correct number of reads to do here is determined first by reading the event size fifo corresponding to the GEM channel of interest.

Bits	Description
15:0	GEM EventData word